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AUTHORITY

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AD 275 708

ENGINEERING SERVICES ON
TRANSISTORS

REPORT NO. 7

SECOND QUARTERLY PROGRESS REPORT

PERIOD COVERED: 1 OCTOBER TO 31 DECEMBER 1961
DATE OF THIS REPORT: 31 MARCH 1962

Contract DA 36-039 sc-88931
(Continuation of Contract DA 36-039 sc-88962)
File No. 00523-PM-62-91-91 (4905)
DA Project No. 3A-99-21-001

U. S. Army Signal Research and Development Laboratory
Fort Monmouth, N. J.

Prepared by Bell Telephone Laboratories, Incorporated
On behalf of Western Electric Company, Incorporated
222 Broadway, New York 38, N. Y.

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U.S. Army Signal Research and Development Laboratory
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OBJECT

The general objective of this contract is to make studies and investigations related to transistors and transistor-like devices, together with their circuit properties and applications, with a view toward demonstrating and increasing the practicability of their use in operating equipment.

This report was prepared by Bell Telephone Laboratories, Incorporated
On behalf of Western Electric Company Incorporated
222 Broadway, New York 38, N. Y.

The following engineers and scientists participated in its preparation:

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SUMMARY OF STATUS

Work on this contract is a continuation of that carried out on Contracts DA 36-039 sc-88962, DA 36-039 sc-85352 and earlier contracts of this continuous series.

Status of Tasks 4 and 9 is summarized below. Tasks 1, 2, 3, 5, 6 and 8 have been completed as reported previously under earlier contracts. Task 7 is inactive by mutual agreement. A final report is being prepared on task 2.

During the period covered by this report, 1 October to 31 December 1961, approximately 2000 engineering man-hours were devoted to work on this contract.

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Work has continued on the 1-watt, 1000-mc transistor. The principal effort has been directed toward fabrication of the new structure which was described in the last report. This structure uses oxide masking for defining the collector junction and for separation of the base and emitter electrodes. Evaporation masks for this structure have been completed and have proven satisfactory. Several evaporation runs have been made and problems associated with the new structure are being worked out. Test transistors of the mesa structure with 1 x 20 mil emitter and base electrodes have also been fabricated during this quarter. Characterization studies of the transistor have continued. Improvement in the collector junction breakdown voltage and reduction of the encapsulation parasitic inductances are necessary to meet the objectives. Solutions to these problems are being sought.

Design calculations have been carried out for a low-power transistor to be used in the low microwave frequency range. A unilateral gain of 14 db at 3 kmc is indicated for the device. The transistor uses a dot emitter 0.25-mil in diameter and a ring base contact, separated from the emitter by 0.1 mil. The technique of oxide masking for the collector junction and of oxide separation of the emitter and base electrodes is also used for this transistor. We have attempted to fabricate the structure, and the very small geometry has been obtained. However, scattering of the evaporated materials during the evaporation of the oxides and electrodes presents a serious problem. The necessary improvements in evaporation techniques to reduce the scattering are being investigated.

A study of the problem of the origin of the base current in diffused-base germanium transistors has been carried out. Experiments have shown that the low-frequency base current is the result of a surface recombination within the emitter space-charge region at the perimeter of the emitter electrode. This current appears to be responsible for the fall-off of the low-frequency current gain of all diffused-base germanium transistors at low emitter currents. Further experiments are in progress to determine how this recombination current can be reduced.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Work is continuing on the development of the technology necessary for the production of integrated circuits. In conjunction with this, the terminal properties of variations of standard logic circuits are being studied.

Surveys have been made in an attempt to define the optimum method of integration.

Accelerated aging techniques are being applied to investigate various particular mechanisms of failure associated with integrated devices. Mechanisms of failure concerning the leads and contacts to the devices are being studied directly, through the use of particular test vehicles.

A final series of accelerated aging tests are being carried out on multiple diodes in a single encapsulation. These tests involve both thermal and electrical stresses.

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LIST OF ILLUSTRATIONS

SECTION 1 - PURPOSE

The general purpose of this contract is to make studies and investigations related to transistors and transistor-like devices, together with their circuit properties and applications, with a view toward demonstrating and increasing the practicality of their use in operating equipment. This contract is a successor to preceding contracts of a similar nature: Contract W36-039 sc-44497, Contract DA 36-039 sc-5589, Contract DA 36-039 sc-64618, Contract DA 36-039 sc-85352, and Contract DA 36-039 sc-88962.

These contracts call for services, facilities, and material to be employed on mutually acceptable tasks. Of the nine tasks assigned, five have been completed with final reports. Work on Task 2, Transistor Reliability was terminated in August 1961. A final report is being prepared. Brief descriptions of other tasks and dates of Final Reports are contained in Section 1 of Report No. 6 dated 31 December 1961, the First Quarterly Report issued under the present contract.

Tasks currently active under this contract are outlined below.

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

The contractor shall make theoretical and experimental studies leading to exploratory models and, upon mutual agreement, to feasibility designs of:

1. New transistors using new or previously untried principles.
2. New transistors obtained by studied modifications of existing types.

The new transistors shall be primarily intended and suitable for application to voltage, current, and power amplifiers, and to associated electronic transducers.

In general, transistors having ac amplifying properties in the following ranges are of particular interest:

1. Germanium transistors from 1000 mcps to 3000 mcps with as large power ratings as the state of the art permits.
2. Silicon transistors from 100 mcps to 1000 mcps with as large power ratings and as high temperature ratings as the state of the art permits.
3. Devices of other materials with specific attention to obtaining frequency, power, noise, or temperature advantages over germanium and silicon devices.

TASK 4A - MICROWAVE TRANSISTOR

The Contractor shall conduct a study and investigation leading to the design and fabrication of a transistor capable of operating with a minimum of 10-db gain at 3000 mc. The transistor structure should be of a diffused base mesa type with stripe emitter and base electrodes or with dot emitter and ring base electrodes. An accurate design theory for such a device shall be established together with an appropriate equivalent circuit including package parameters. It is desired that the transistor be matched into 50-ohm input and output coaxial terminations. From a microwave point of view the structure (package and transistor) shall be basically broadband. Ideally, the transistor should be capable of greater than 10-db power gain from d.c. to 3000 mc. Appropriate experimental models of such devices including any necessary adapters, indicative of the progress made shall be furnished during the course of this program.

TASK 4B - 1000 MC, 1 WATT TRANSISTOR

The Contractor shall conduct a study and investigation leading to the design and fabrication of a transistor capable of operating with a minimum of 1 watt of power output at 1000 mc with a minimum gain of 10 db and with a minimum efficiency of 30 per cent, for this power output and gain. An accurate design theory for such a device shall be established together with an appropriate equivalent circuit including package parameters. The structure shall be an hermetically sealed package with provisions for mounting on simple heat sinks. Appropriate experimental models of such devices, including any necessary adapters, indicative of the progress made shall be furnished during the course of this program.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

The Contractor shall make theoretical and experimental studies leading to exploratory models, and upon mutual agreement, to feasibility designs and finally to development models of semiconductor components able to perform more complex functions than existing components can, thereby reducing the number of components needed in electronic systems with the ultimate objective of improving the reliability and reducing the cost of such systems. The components to be investigated shall include:

1. Functional devices, namely devices designed from physical phenomena to perform as directly as possible desired systems functions.

2. Diodes and transistors in miniature insulated packages to be compatible with thin film resistor-capacitor techniques. These packages may form an integral part of an insulating substrate on which resistive and capacitive films may be evaporated to form complete circuits.

3. Integrated circuits, namely combination of circuit elements including, where appropriate, functional devices designed and fabricated as units to perform desired systems functions.

The work shall include but not be limited to:

1. Evaluation of systems requirements and related components requirements with attention to such figures of merit as speed, gain, power dissipation, impedance,

reliability, packing density, interconnection topology, etc. A study shall be undertaken of selected categories of semiconductor components to determine their universality with respect to a variety of systems. For example, integrated diode-transistor logic circuits shall be studied for gating and flip-flop circuits. The gating circuits studied shall be designed for optimum fan-in, fan-out requirements. The fan-in, fan-out requirements should be based upon systems analysis.

2. Study of miniature diodes and transistors in insulated packages shall be undertaken to determine the effects, if any, of the packaging techniques on the performance and reliability of these devices. Wherever possible, comparative conventional devices shall be used to make this analysis most meaningful.

3. Fabrication of these selected exploratory components and circuits to determine their figures of merit. For example, four-layer, three-terminal device structures (PNPN) having turn-off gain properties shall be investigated for application to functional circuits. In addition, the contractor shall endeavor to determine the reliability inter-relationship of several semiconductor devices (i.e. diodes and transistors) contained in a common sealed package or several junctions fabricated in a common semiconductor wafer.

4. The cost factors associated with all of the above shall be investigated, particularly with respect to yield on multiple devices in common package or multiple junctions within one wafer.

SECTION 2 - ABSTRACT

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

A proposed germanium diffused-base transistor, intended for use as an amplifier in the low microwave frequency range, is described and discussed in Chapter 1. The transistor has a circular emitter of 0.25-mil diameter, a ring base electrode, and a circular collector of 1-mil diameter defined by an oxide ring. From an equivalent circuit for the transistor, the short-circuit admittance parameters are calculated as a function of frequency, and unilateral gain is calculated as a function of frequency. At 3 Gc, the calculated unilateral gain is 14 db for a bias of V_{CB} = 5 v, I_e = 2 ma. The need for a new header with lower series lead inductance than the M2174 header is discussed.

Two germanium processing changes are described. The first, a change in the base-layer diffusion, is a method for lowering the series base resistance using two diffusions with different surface concentrations and different diffusion depths. The second, a change in the evaporation of emitter and base contacts, allows the evaporation of circular contacts. Some initial evaporation results are presented.

Chapter 2 describes work on the M2260 transistor designed for 1-watt power output at 1 kmc. The specific dimensions and diffusion data are presented for a transistor using the oxide-spaced interdigitated structure outlined in the last report. The predicted values of the equivalent circuit parameters based on these dimensions are given. The preliminary evaporations using the new masks have been carried out, and provide the desired structure within tolerance limits.

Three-stripe mesa units with 1 x 20 mil stripes have been used for electrical characterization. The calculation of r_b' from the high-frequency h_{ib} measurements was not possible due to excessive header input inductance. The value of r_b' calculated from low-frequency h_{ib} and α measurements is at least as low as that predicted from the structure. These units provided a small-signal power gain of 20 db at 1 kmc with zero db reverse transfer, in a tuned-input tuned-output amplifier with no external feedback.

Chapter 3 treats the surface dependence of the dc and low-frequency base current in germanium diffused-base transistors. The base current in germanium diffused-base transistors has a dependence on emitter-base voltage and on temperature which is shown to be in quantitative agreement with the theory of recombination at traps within the emitter space-charge with energy near the mid-gap. However, as pointed out by Moll, the trap density required in this model is so high that a homogeneous distribution of such traps in the base region near the emitter barrier is inconsistent with the high gain observed.

The base current is also found to be strongly surface dependent. Common-emitter current gain can be cycled repeatedly, such that it changes by factors of

order ten. Washing in water is used to decrease base current; baking in dry hydrogen to increase it. The base current under reverse emitter-base voltage shows, quantitatively, the same surface dependence as that seen under forward bias.

These results suggest that base current in these transistors is dominated by recombination at surface traps within the emitter space charge. A contribution to the base current in silicon planar transistors arising in a similar way has been suggested by Sah.

The data suggest that the emitter at the surface at equilibrium has a configuration like a junction between p and n regions, both lightly doped, and that surface recombination velocity is high.

The single-trap approximation gives a trap 80 mv from the mid-gap. The traps are thought to be characteristic of the Ge-Ge oxide interface and to be deactivated by the presence of water.

When a transistor which has been washed in water is later baked in hydrogen, the same trap persists, its density increases, and the surface positive charge also increases.

Collector current depends on emitter-base voltage and temperature as expected from ideal pn junction theory and is nearly independent of surface treatment. The different dependence of base and collector current on emitter-base voltage results in the well-known dependence of common-emitter current gain on current. The model is believed to apply to germanium high-frequency, high-gain transistors which show $I_B \propto \exp\left(\frac{qV_{EB}}{1.5kT}\right)$, which includes virtually all currently available types.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Chapter 4 is an interim report on the accelerated aging experiments being carried out with multiple diodes in a single encapsulation. The results show that the main population, consisting of about 90 per cent of the devices, possess good tolerance to both electrical and thermal stress.

Chapter 5 presents a review of the merits and defects of various approaches to integrated semiconductor circuits. It is concluded that most gains are obtained through a flexible approach, using multiple like devices on a common substrate and the common encapsulation of unlike devices on separate substrates.

Chapter 6 discusses the effect of temperature aging on thermal compression bonded contact between leads wire of various metals, and an aluminum contact on a semiconductor device. The result shows that the resistance of the bond increases until an open circuit occurs.

SECTION 3 - PUBLICATIONS AND REPORTS

"A paper by J. T. Nelson and A. G. Foyt," "Germanium Transistors for Operation above 1 kmc," was presented at the meeting of the Professional Group on Electron Devices of the IRE held in Washington D.C. on October 26, 1961.

SECTION 4 - FACTUAL DATA

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Chapter 1

THE M2275, A GERMANIUM MICROWAVE TRANSISTOR WITH CIRCULAR ELECTRODES

By. A. G. Foyt

1.1 INTRODUCTION

This chapter discusses a proposed germanium diffused-base transistor intended for use as an amplifier in the low microwave frequency range. The transistor has circular emitter and base contacts and a circular collector defined by an oxide ring. The transistor has a calculated unilateral power gain of 14 db at 3 Gc when operated at a 10-mw bias level. An equivalent circuit for the transistor is presented, and the two-port parameters of the equivalent circuit are computed as a function of frequency. Unilateral gain, as defined by S. J. Mason, is computed from the two-port parameters and is shown as a function of frequency. Finally, two changes in the germanium processing, the diffusion of the base layer and the evaporation of the surface contacts, are discussed.

1.2 STRUCTURE OF THE TRANSISTOR

This transistor is to be a germanium pnp diffused-base transistor. It is designed for use as a common-base amplifier in the low microwave frequency range. A similar transistor, the M2174, a germanium diffused-base mesa transistor with stripe emitter and base contacts has shown useful performance as an amplifier in the upper UHF range. The new structure is basically an attempt to reduce the size of the M2174 and improve the performance at high frequency.

However, an attempt to reduce the size of the M2174 by a reduction of all dimensions does not seem feasible. The emitter and base stripe widths are found to be the smallest size for which evaporation masks can be made reproducibly by present techniques, so a reduction in stripe width could not be made. If, however, this dimension is held fixed, the size of the transistor can be reduced by reducing the length of

the emitter and base stripes. This length can be reduced until the emitter and base contacts are square. However, as shown by Early (Ref. 1) this reduction does not improve the gain-bandwidth product. If, however, the base contact is made as a ring around the emitter, the series base resistance will be reduced with no increase in the collector capacity under the emitter, and the gain-bandwidth product will be increased. In the final design a ring was used for the base contact and a circular dot was used for the emitter contact.

With a ring-dot contact geometry, a circular collector would minimize the collector area. Since the collector area outside the base contact does not contribute to the transistor action and is, in fact, an unwanted parasitic capacity, the transistor was designed to make this area small. An oxide mask that would define the collector-base junction seemed to be the most suitable method for controlling the collector area (Ref. 2). By defining the collector junction with an oxide mask and by laying part of the base ring on this oxide mask, the collector area can be reduced by factors of four or more over the M2174 design. Finally, the method used to limit the collector area was used to limit the emitter area.

Using the ideas discussed above, the transistor was designed as shown in Fig. 1.

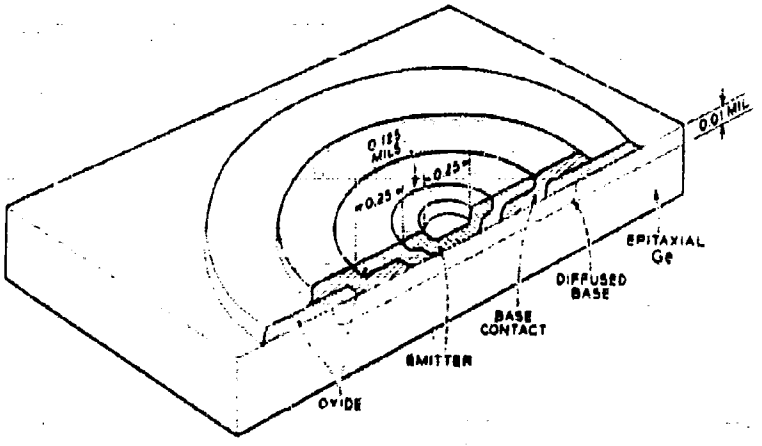

Fig. 1 - Proposed new structure for the 10-milliwatt common-base amplifier

1.3 ELECTRICAL EVALUATION OF THE PROPOSED TRANSISTOR

Electrical evaluation of this transistor design is based on an equivalent circuit for the transistor. In this section, a set of two-port parameters and unilateral gain are computed from the equivalent circuit.

A similar equivalent circuit was used previously in evaluating the M2174 transistor. The circuit consists of a "T" equivalent circuit for the germanium wafer with the header equivalent circuit located around the outside of "T". The complete circuit with element values is shown in Fig. 2. The element values shown were calculated, measured, or estimated from previous experience with similar transistors, as itemized :

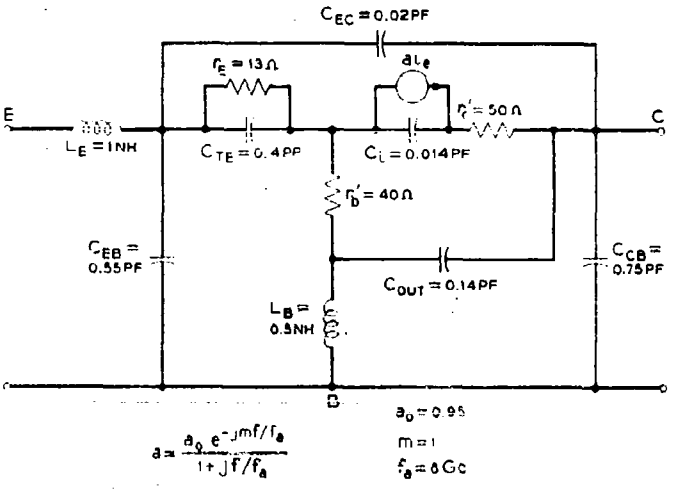

Fig. 2 - Equivalent circuit for the M2275 transistor

1. a - Thomas and Moll (Ref. 3) have shown that the common-base current transfer ratio a is given for most transistors by

$$a = \frac{a_0 e^{-jmf/f_a}}{1 + jf/f_a},$$

where a_0 is the low-frequency current gain, f_a is the frequency at which $|a|$ is down three db from its low-frequency value, and m is the excess phase constant.

2. f_a - Early (Ref. 4) has shown that the common-emitter unity gain frequency f_t, where

$$f_a = f_t (1 + a_0 m),$$

can be calculated as a sum of four time constants,

$$\frac{1}{2\pi f_t} = \tau_{ec},$$

where

$$\tau_{ec} = \tau_e + \tau_b + \tau_c + \tau_x .$$

τ_e = the time constant for the emitter diode,

$$\tau_e = r_e C_e$$

τ_b = the base transit time,

$$\tau_b = \frac{w^2}{3D} ,$$

where w is the base width and D is the diffusion coefficient for holes in the base layer.

τ_c = the time constant for the collector resistance-collector capacity,

$$\tau_c = r_c' C_l .$$

τ_x = the time constant for a hole crossing the collector-barrier region,

$$\tau_x = \frac{x}{2V_L}$$

where x is the collector-barrier width, and V_L is the limiting velocity for holes in germanium.

These time constants are shown as a function of C_o, the base-layer surface concentration, in Figs. 3 and 4 for two levels of collector doping.

3. a_o and m were estimated from previous experience on the M2174.

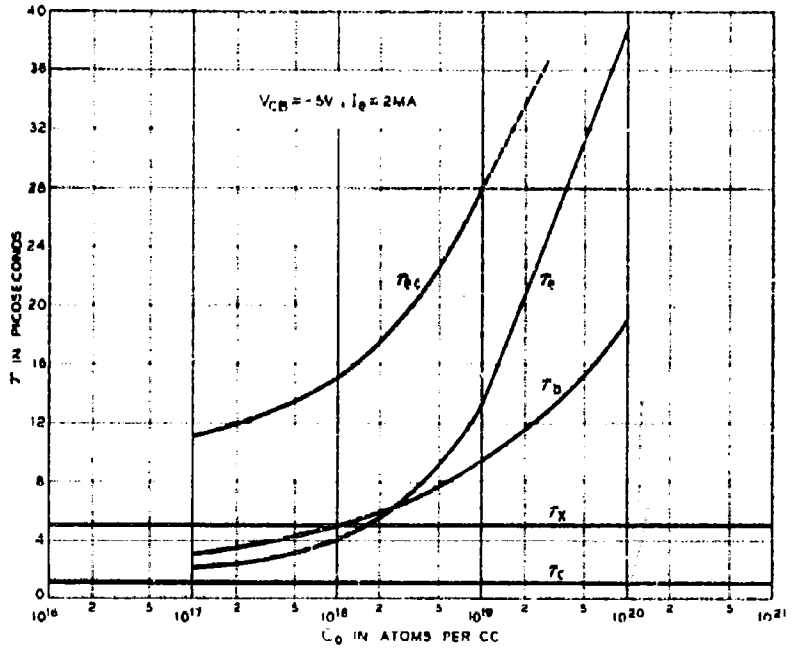

Fig. 3 - Computed time constants vs. base layer surface concentration for collector doping of 5 x 10^{16}

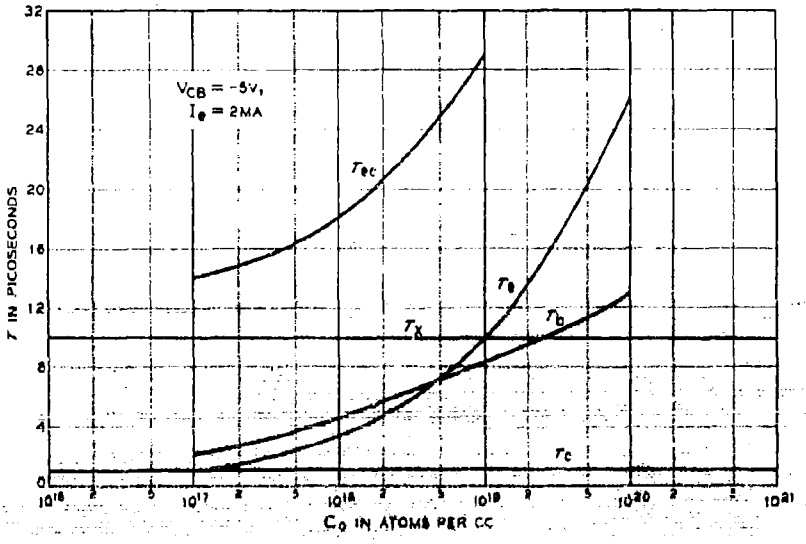

Fig. 4 - Computed time constants vs. base layer surface concentration for collector doping of 10^{16}

4. C_{out} and C_i, the collector outer and inner capacities, were calculated using the data for diffused junction capacity computed by Lawrence and Warner (Ref. 5).

5. r'_b, the series base resistance, was computed using a method which Early (Ref. 6) applied to alloy junction transistors,

$$r'_b = \frac{\rho_{s1}}{8\pi} + \frac{\rho_{s2}}{2\pi} \ln \frac{r_2}{r_1},$$

where ρ_{s1}, ρ_{s2} are the sheet resistances of the base layer under the emitter and between the emitter and base contacts respectively, r_1 is the radius of the emitter contact, and r_2 is the radius of the base contact.

6. r_e = emitter diode resistance = $\frac{kT}{qI_e}$.

7. C_e = emitter diode capacity.

8. r'_c = the collector series resistance and was estimated from the M2174 transistor.

9. L_c, L_b = the series header inductances. The values shown were measured for the M2174 coaxial header.

10. C_{eb}, C_{bc}, C_{eo} = the shunt header capacities. The values shown were measured on the M2174 coaxial header.

A C_o of 2×10^{18} was chosen for this transistor as a reasonable compromise between series base resistance and α_o. A collector doping of 5×10^{16} was chosen as a compromise between frequency performance and collector breakdown voltage. From this equivalent circuit, a set of two-port parameters, the short-circuit parameters, were calculated using an IBM 650 computer. The parameters versus frequency figures are shown in Figs. 5 through 8.

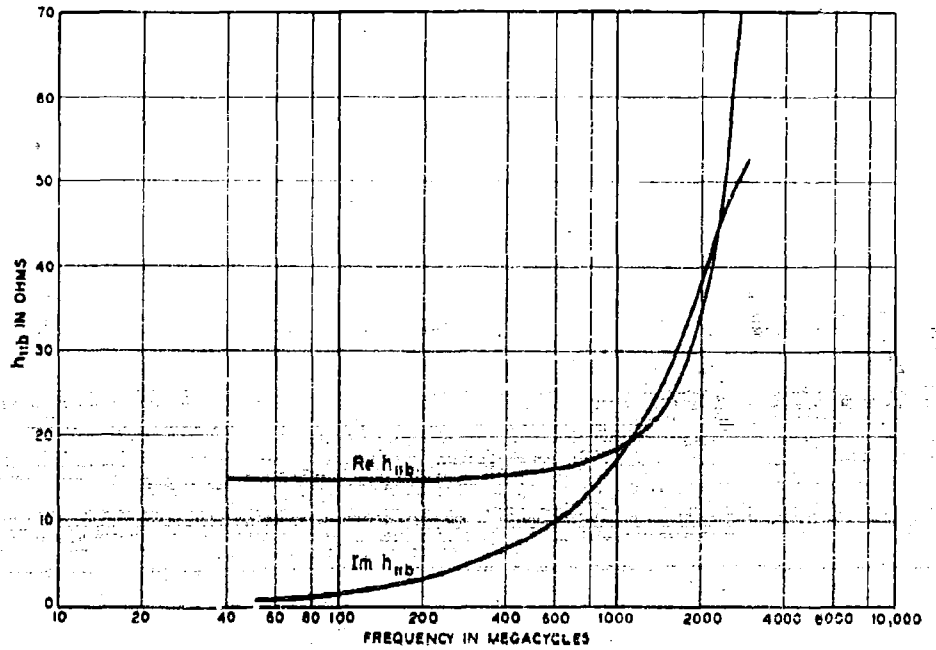

Fig. 5 - $h_{11b} = 1/y_{11b}$ vs. frequency
(Computed from equivalent circuit)

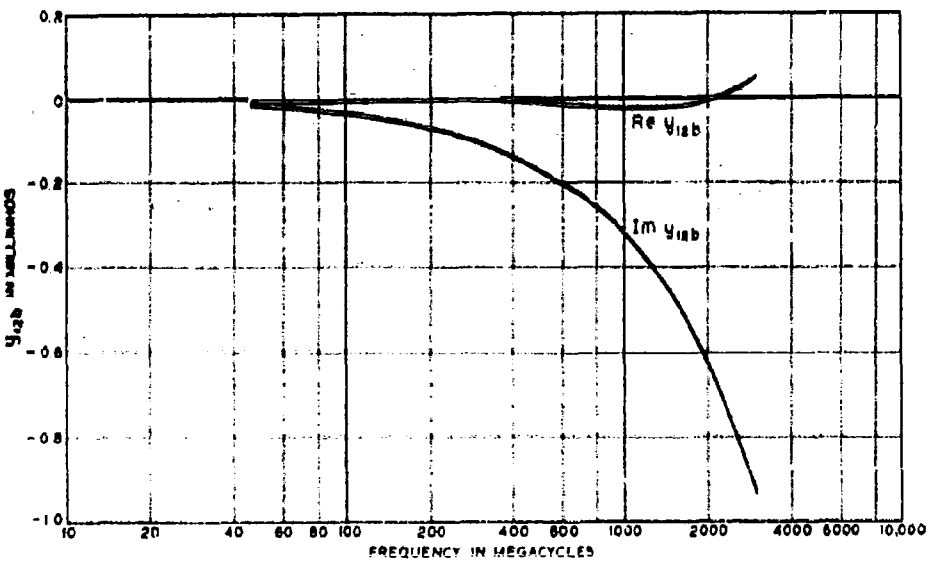

Fig. 6 - y_{12b} vs. frequency
(Computed from equivalent circuit)

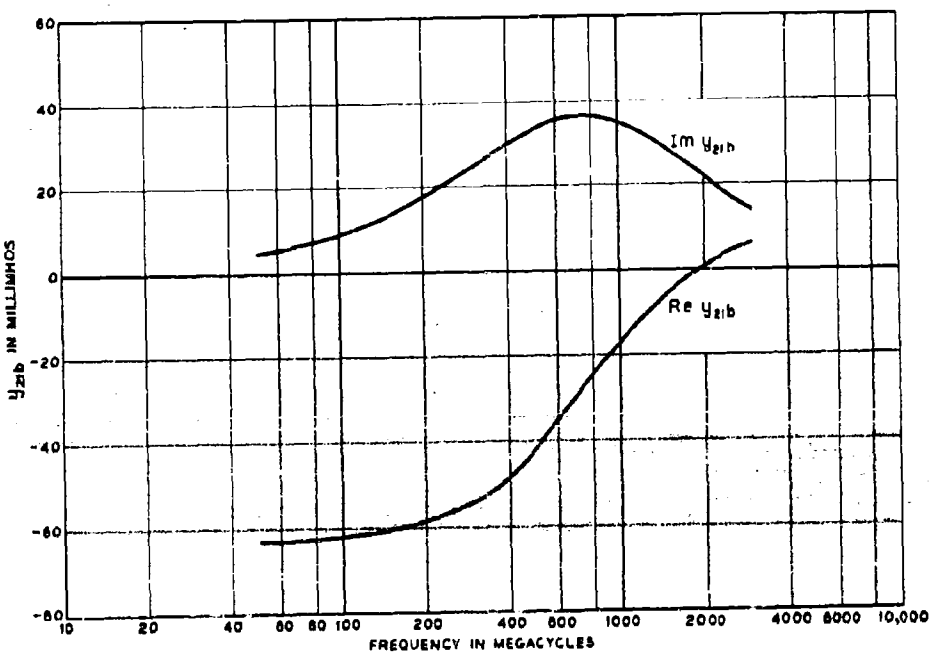

Fig. 7 - y_{21b} vs. frequency
(Computed from equivalent circuit)

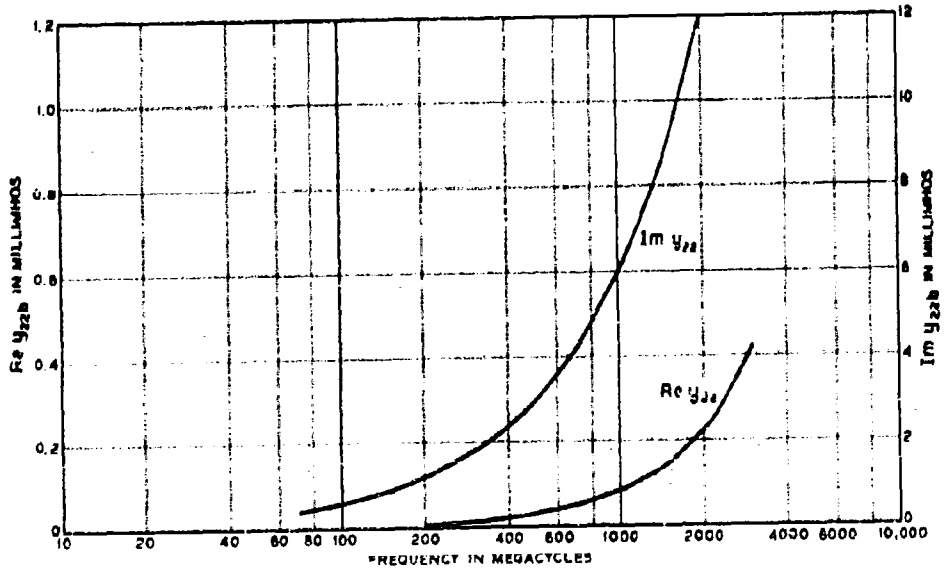

Fig. 8 - y_{22b} vs. frequency
(Computed from equivalent circuit)

From the computed y parameters, several measures of performance may be calculated for the transistor. A measure that has been commonly used in transistor evaluation is Unilateral Gain (Ref. 7) defined by S. J. Mason as

$$U = \frac{|\, y_{12} - y_{21} \,|^2}{4[\, re(y_{11})re(y_{22}) - re(y_{12})re(y_{21})\,]} .$$

U is shown by Mason to be the maximum neutralized power gain for the transistor in a lossless, passive, reciprocal tuning and neutralizing network. For this transistor U versus frequency is shown in Fig. 9.

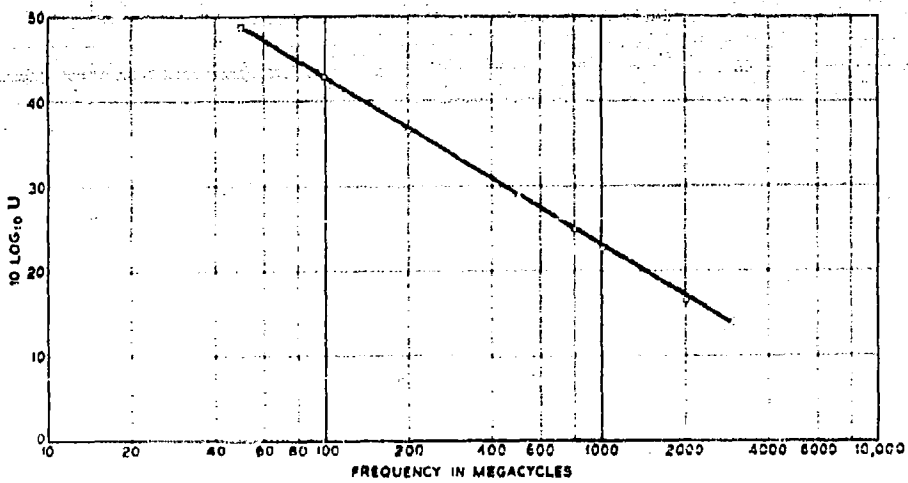

Fig. 9 - Unilateral gain vs. frequency
(Computed from equivalent circuit)

1.3.1 Discussion of the Two-Port Calculations

Several observations of electrical evaluation can be made at this time. First, the calculation of f_a was shown for the M2174 to give a value that was two to three times higher than the observed value. For the M2275 the calculated value was reduced by a factor of three for the equivalent circuit. Second, the calculated input impedance, y_{11}^{-1}, is increasing rapidly at 3 Gc, the highest frequency of calculation. Part of this increase is due to header inductance. To reduce this resonance effect in input impedance, a lower inductance coaxial header will be used for this transistor. Finally, the short-circuit output admittance is very low, so that a low loss impedance matching section must be used to match the output. Our experiments on coaxial lines indicate that such a matching section can be built.

1.4 NEW GERMANIUM PROCESSING

Two departures from previous techniques will be made in the germanium processing for this transistor. The first departure is a method for contouring the base-layer impurity profile using two separate diffusions to lower the series base resistance. The second departure is a method for evaporating the circular emitter and base contacts.

The method for lowering the series base resistance is illustrated by the impurity profile of the base layer, Fig. 10. As shown, there are two separate diffused layers. The first diffusion, with lower C_0 and lower diffusion coefficient, extends the entire base-width and provides base doping under the emitter. The second diffusion, with higher C_0 and higher diffusion coefficient, extends to the emitter penetration depth, and lowers the series base resistance between the emitter and base contacts.

This method provides independent control of the doping under the emitter and the doping the emitter and base contacts. Since the area between the emitter and base is only series resistance, it will be doped as heavily as possible. The doping under the emitter partially determines the α_0 of the transistor and determines the base resistance under the emitter. A compromise must be made between α_0 and base resistance. From experience with the M2174, a base-layer depth of 1/4 micron and a C_0 of 2×10^{18} is a reasonable compromise between α_0 and r_b'.

The second departure from standard processing is the method of evaporating emitter and base contacts and the oxide layers. On previous transistors the emitter and base contacts were evaporated by shadow masking of the evaporated material using a metal mask clamped over the germanium in a stationary holder. For the M2275 a shadow masking technique will be used. However, the holder will be allowed to rotate for the evaporation of a ring and will be allowed to tilt for control of the ring diameter. A similar method of evaporation has been reported by Wiegmann (Ref. 8). This technique is not completely controlled at this time, and the

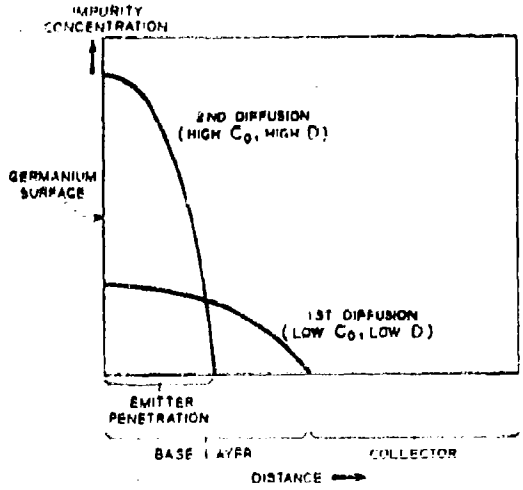

Fig. 10 - Base impurity concentration vs. depth

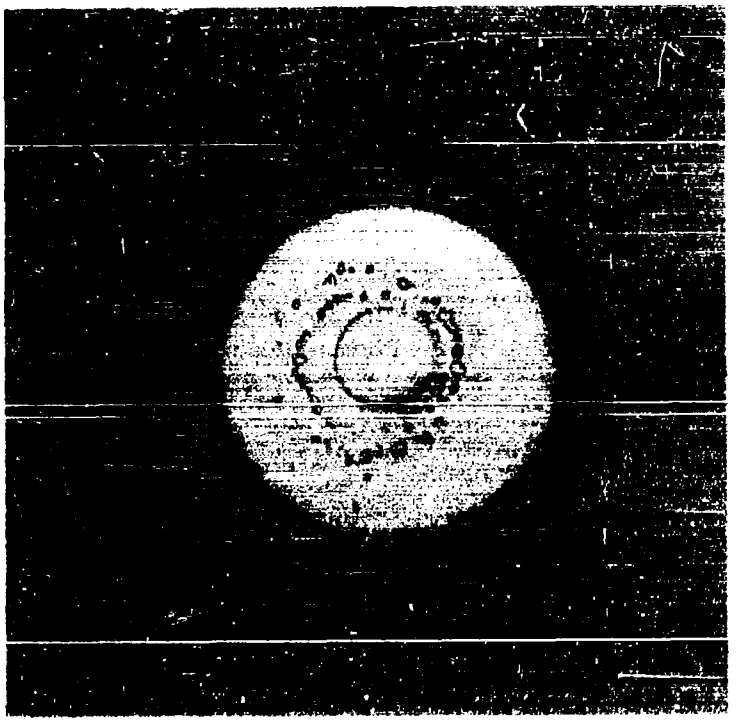

Fig. 11 - Initial ring-dot evaporations

details of the evaporation process will be reported at a later date. However, some initial results indicate that the method does work. Some of the first evaporations are shown in Fig. 11.

1.5 SUMMARY

A proposed germanium diffused-base planar collector transistor has been presented and described. The transistor has been calculated to be capable of 14 db unilateral gain at 3 Gc when operated at the design bias level of V_{CB} = 5V, I_e = 2 ma. An examination of the transistor input impedance shows the need for a new header with lower series inductance than the M2174 coaxial header. An examination of the transistor output impedance shows the need for a low-loss matching section to match the output impedance to standard coaxial line. Our experiments indicate that such a matching section can be built. Two germanium processing changes have been presented, one for lowering the base series resistance, and one for evaporating the surface contacts on the proposed transistor. Initial results indicate the transistor can be made.

REFERENCES

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Chapter 2

STATUS OF THE M2260, 1-WATT, 1000-mc TRANSISTOR

By R. E. Davis

2.1 INTRODUCTION AND SUMMARY

The M2260 is a p-n-p diffused-base transistor designed for 1-watt power output at 1 kmc. The principal effort during this period has been devoted to the fabrication of the oxide-separated interdigitated structure. Initial evaporations using new masks have provided the desired structure within the allowable tolerances.

Some small-signal measurements have been obtained on 1 x 20 mil 3-stripe mesa units. The values of r_b' calculated from the low-frequency h_{fb} and α measurements are at least as low as those calculated from the structure. The calculation of r_b' from the high-frequency h_{fb} measurements was not possible, due to excessive header inductance in the input lead. These units provided a small-signal power gain of 20 db at 1 kmc, with reverse transfer of 0 db, in a tuned-input tuned-output amplifier with no external feedback.

This chapter gives the design dimensions and calculated parameter values for a 1-watt, 1-kmc transistor using the oxide-spaced structure.

2.2 DIMENSIONS AND PARAMETER VALUES FOR A 1-WATT, 1-kmc TRANSISTOR USING THE OXIDE-SPACED INTERDIGITATED STRUCTURE

A description of this structure and its inherent advantages has previously appeared in these reports (Ref. 1). Such a transistor structure is shown in Fig. 12. The dimensions given in Table 2-1 are based on the requirements of 1 watt output power at 1 kmc. The starting material is 0.5 Ω-cm p-type epitaxial germanium deposited on 0.01 Ω-cm p-type substrate. The base diffusion depth is 0.3 micron and the emitter is assumed to penetrate 0.1 micron, which represents the best estimate based on previous experience. The base sheet resistance for three different values of diffusion surface concentration is given in Table 2-2 for the case of antimony diffusion alone, and also for the case of antimony diffusion followed by an arsenic diffusion whose sheet resistance is 250 Ω/□ (Ref. 2). The values of r_b' for this structure based on these sheet resistances are also given in the table. Table 2-3 gives the theoretical values of the significant parameters, based on the dimensions shown in Table 2-1 and the diffusion parameters shown above. Some of the capacities appearing in this table are not found in the mesa structure. These parasitic capacities, identified by primes, are the capacities of the oxide separated lead materials

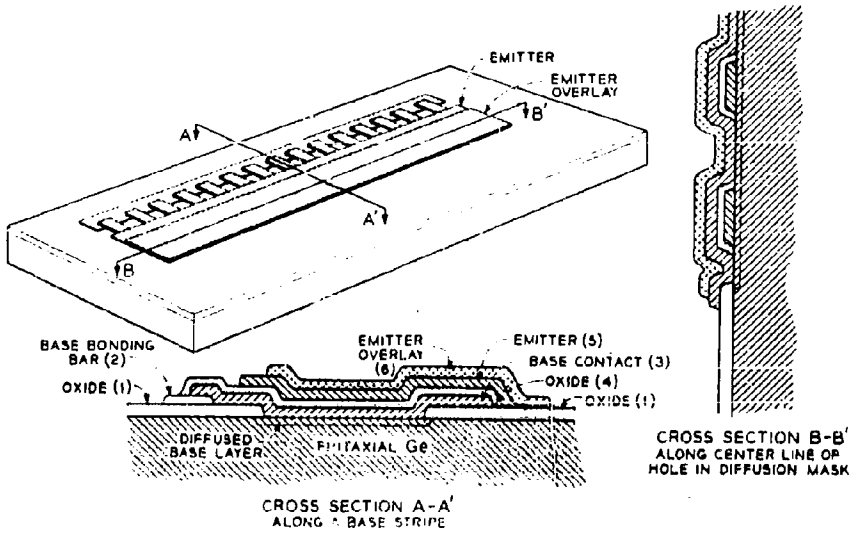

Fig. 12 - Oxide-spaced interdigitated structure

Table 2-1

DIMENSIONS FOR A 1-WATT, 1-kmc, OXIDE-SPACED TRANSISTOR

Reference No. in Fig. 12 and Description	Dimensions (in mils)	
	Length	Width
(1) Hole in SiO layer	20	4.5
(2) Base lead bonding bar	23	2.0
(3) Base contact stripes	8.5	0.6
(4) Oxide coating on base stripes	8.9	1.0
(5) Emitter contact	23	6.5
(6) Emitter overlay	23	6.5
Base-stripe overlap on base bonding bar		1.0
Distance between base bonding bar and oxide hole		2.0
Distance between base bonding bar and edge of emitter contact		1.0
Displacement of emitter overlay w.r. to emitter contact		1.0

Table 2-2

r_b' AS A FUNCTION OF DIFFUSED-BASE LAYER PARAMETERS

Diffusant Surface Concentration (cm^{-3})		$\bar{\sigma}$ B $(\Omega\text{-cm})^{-1}$	$\bar{\sigma}$ E $(\Omega\text{-cm})^{-1}$	R_{SB} Ω/□	R_{SE} Ω/□	r_b' (ohms)
$C_o = 10^{18} S_b$		58	30	575	1670	2.61
	+250Ω/□ As			174	1670	1.87
$C_o = 2 \times 10^{18}$		85	42	392	1190	1.83
	+250Ω/□ As			153	1190	1.38
$C_o = 3 \times 10^{18}$		110	52	300	1000	1.46
	+250Ω/□ As			136	1000	1.18

$\bar{\sigma}_B$ = average conductivity in base layer

$\bar{\sigma}_E$ = average conductivity under emitter

R_{SB} = sheet resistance of base

R_{SE} = sheet resistance under emitter

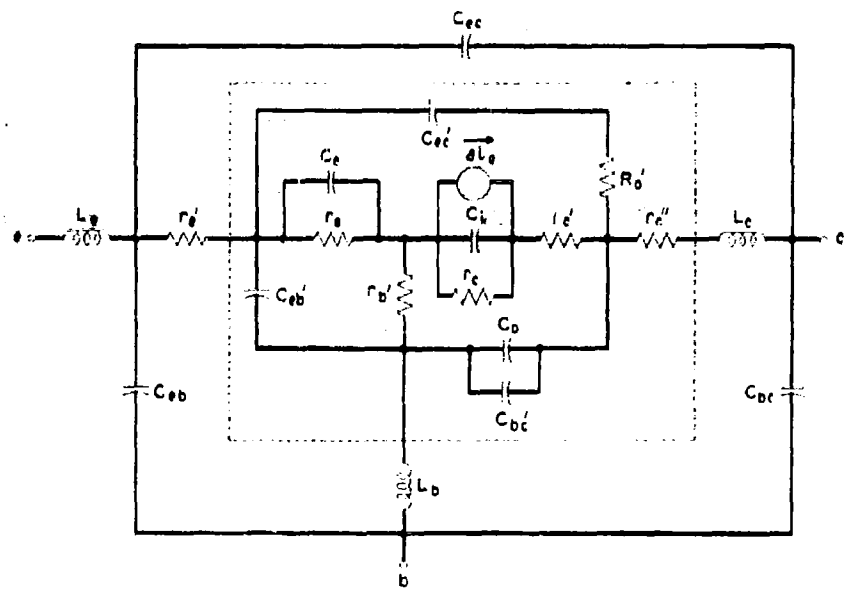

Fig. 13 - Equivalent circuit of the oxide-spaced structure

Table 2-3

EQUIVALENT CIRCUIT PARAMETERS*

Symbol	Description	Value
r'_b	base resistance	See Table 2-2
C_o	outer-collector junction capacity (everywhere except under the emitter)	4.0 pf
C'_{bc}	base contact to collector capacity through the SiO	1.8 pf
C_i	inner-collector junction capacity (under the emitter)	2.2 pf
C_e	emitter transition capacity	50 pf
C'_{ec}	emitter contact to collector capacity through the SiO	1.0 pf
C'_{eb}	emitter contact to base contact capacity through SiO	1.3 pf
r'_c	collector body resistance under the emitter	0.1 Ω
r''_c	substrate resistance under the emitter	0.25 Ω
R'_b	collector body resistance under inactive portion of emitter lead	0.072Ω
f_t	common-emitter unity gain frequency	2 kmc†

* All capacities calculated at 10V collector bias
† Based on M2107 results

and large bonding contacts. The equivalent circuit for the transistor is shown in Fig. 13 with these parasitic capacities included.

2.3 INITIAL EVAPORATION OF THE NEW STRUCTURE

One of the first evaporations using the new masks is shown in Fig. 14. The various parts of the structure may be identified by comparison with Fig. 12. The dark sections on the base stripes, where they contact the germanium, were caused by the base stripes buckling and peeling away from the germanium before alloying. This was probably due to the germanium surface condition, since subsequent slabs which were cleaned before evaporation have not exhibited this behavior. The structure was well within tolerance limits on the first few evaporations, however, in subsequent evaporations the stripes have been misplaced due to a malfunction of the jigs. The jigs are now being modified to correct this shortcoming. No units have been satisfactory for electrical testing to date.

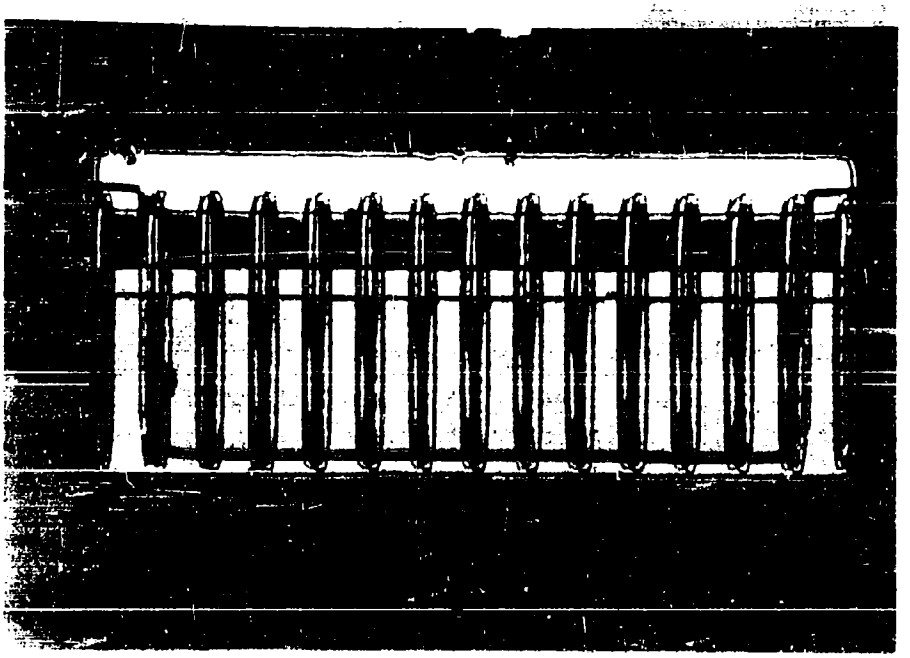

Fig. 14 — Evaporated oxide spaced structure

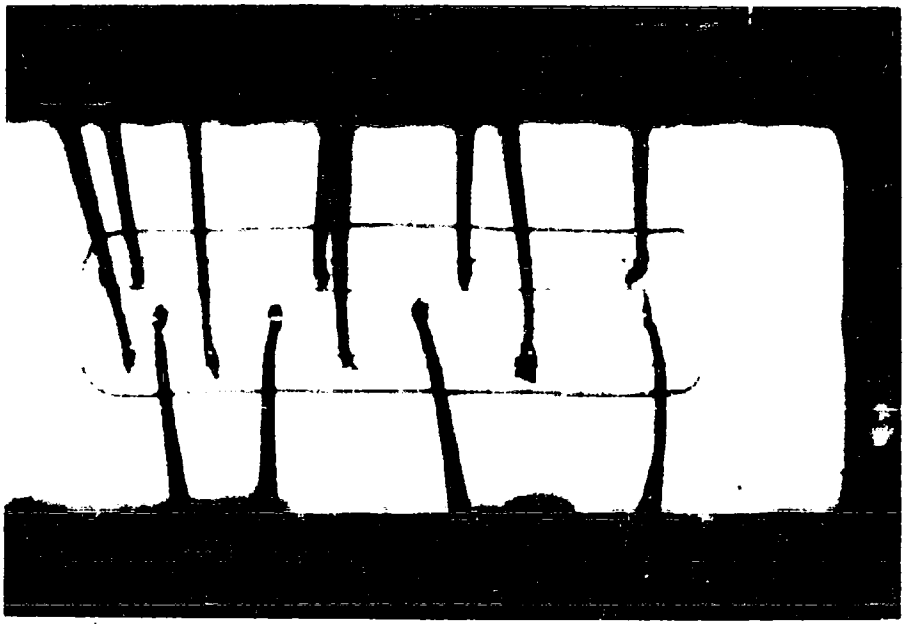

Fig. 15 — Three-stripe mesa transistor after bonding

Table 2-4

LOW-FREQUENCY α AND h_{ib} MEASUREMENTS

Bias		Unit	α	h_{ib}	($r'_e = 0$)	($r'_e \neq 0$)	
I_e (ma)	V_{cb} (volts)	No.		(ohms)	r'_b (ohms)	r'_b (ohms)	r'_e (ohms)
50	2.5	1	0.9588	0.854	8.11	2.40	.235
50	2.5	5	0.9669	0.855	10.1	4.20	.196
50	2.5	7	0.9599	0.873	8.80	3.74	.203
100	2.5	1	0.9696	0.568	10.2	r'_b (Theoretical)	
100	2.5	5	0.9750	0.561	12.0	= 12 ohms	
100	2.5	7	0.9698	0.576	10.5		

2.4 SMALL-SIGNAL MEASUREMENTS ON MESA UNITS

Three 3-stripe mesa units with 1 x 20 mil stripes, mounted in coaxial headers, were electrically tested. One of these units, after bonding, is shown in Fig. 15. The small-signal low-frequency measurements of h_{ib} and α obtained on the Boonton 275-A transistor test set are given for these units, in Table 2-4. These measurements were taken at two values of emitter current, 50 ma and 100 ma.

The respective values of r'_b were calculated in two different ways for these units. The expression for the short-circuited input impedance of the transistor is given by:

$$h_{ib} = r'_b (1-\alpha) + \frac{KT}{qI_e} + r'_e \ . \tag{1}$$

When the two sets of h_{ib} and α measurements, taken at the two different current levels, are substituted in Equation (1), r'_b is given by:

$$r'_b = \frac{(h_{ib})_1 - (h_{ib})_2 - \left(\frac{KT}{qI_{e1}} - \frac{KT}{qI_{e2}}\right)}{\alpha_2 - \alpha_1}, \tag{2}$$

where the subscript 1 refers to the readings taken at the lower value of emitter current.

Substitution of this value of r'_b in Equation (1) gives r'_e. This solution obviously assumes that both r'_b and r'_e are invariant with change in emitter current.

The values of r_b' calculated from the measurements in this manner appear in Table 2-4 under the column ($r_e' \neq 0$), and are considerably below the theoretical prediction of $r_b' = 12$ ohms.

A second calculation of r_b' was made, assuming that $r_e' = 0$ in Equation (1). These values of r_b' appear in Table 2-4 under the column ($r_e' = 0$). In this case the calculated value of r_b' is closer to the theoretical value, but is different at the two current levels, increasing with an increase in current.

The question as to which of these calculations gives the correct value of r_b' is still not resolved, since there are logical arguments in favor of each case. The increase of r_b' with increase in current, observed for the case $r_e' = 0$, could be explained by an increase in the voltage drop along the emitter stripe with increase in current. On the other hand the lower value of r_b' obtained for the case $r_e' \neq 0$ would be feasible if the $(1 - \alpha)$ current flowing in the base originated at the edge of the stripe, as experiment has indicated (Ref. 3). Under this condition, the theoretical value of r_b' would be 3.23 ohms, which agrees reasonably with the measurements.

The small-signal high-frequency measurements of h_{ib} taken on the G.R. 1607-A transadmittance bridge are shown in Fig. 16, where the real part of h_{ib} is plotted versus the imaginary part of h_{ib}, in the normal manner. The low-frequency measurement is also included for completeness. It is evident from this curve that the

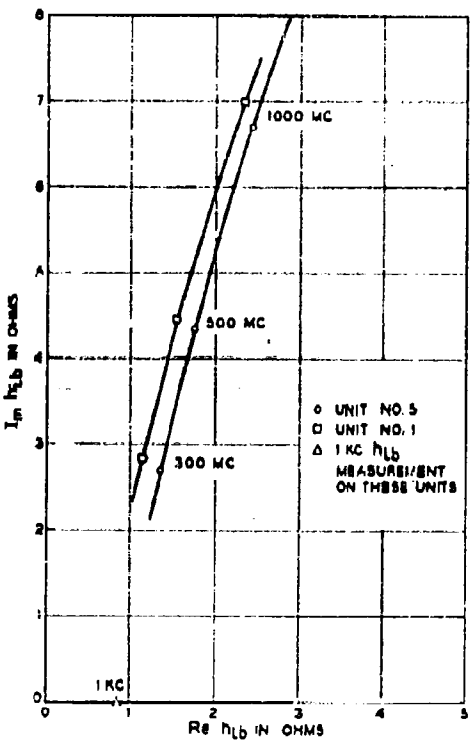

Fig. 16 - High frequency h_{ib} of coaxial M2260 units

Table 2-5

SMALL-SIGNAL GAIN AT 1 kmc

I_e (ma)	V_{cb} (volts)	Forward Gain (db)	Reverse Gain (db)
50	2.5	11.7	-4.3
50	5.0	12.2	-6.4
52	5.0	19.2	-0.8
52	5.0	22.8	+1.7
60	2.5	oscillates	

input inductance of the header completely masks the reactive portion of the transistor input impedance and renders meaningless any deduction of r_b' from these measurements. A new encapsulation is being designed to decrease this header input inductance to a much lower value.

Table 2-5 shows a set of small-signal power gain measurements taken at 1 kmc in a tuned-input tuned-output amplifier with no external feedback. Both the forward and reverse gain have been measured under identical tuning and bias conditions. The maximum forward gain (with reverse gain $\leq$ 0 db) is seen to be approximately 20 db.

2.5 CONCLUSIONS AND PLANS

Preliminary results on the new structure are encouraging and the initial evaporations using the new masks have already given the proper structure, well within tolerances. A slight modification of the evaporation jig should give reproducible results.

The small-signal low-frequency measurements of h_{fb} and α on 1 x 20 mil 3-stripe mesa units give r_b' values at least as low as those calculated from the structure. Calculation of r_b' from the small signal high frequency measurements of h_{fb} was not possible due to excessive input inductance in the header. A small-signal power gain of 20 db at 1 kmc, with reverse transfer of 0 db, was achieved with these units.

Work during the next quarter will be concentrated on producing units with the oxide-spaced structure. Further electrical measurements will be made on these and on 3-stripe mesa units. The low-frequency measurements of r_b' will be further investigated.

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3. A. B. Kuper, this report.

Chapter 3

SURFACE DEPENDENCE OF GERMANIUM HIGH-FREQUENCY, HIGH-GAIN TRANSISTORS

By A. B. Kuper

3.1 INTRODUCTION

The purpose of this investigation is to explore a new surface model of the base current in high-frequency, high-gain germanium (Ge) transistors. Such a transistor implies a thin base and thin emitter both heavily doped, all dimensions very small and lifetime greater than 0.1 μs for minority carriers in the base.

It is well known that ideal pn junction theory based on diffusion and recombination (Ref. 1) does not correctly predict the detailed behavior of transistors (Refs. 2, 3,4). In particular the dependence of current gain on current, $\alpha(I_E)$, and temperature is not explained by analysis based on minority carrier injection and recombination in the emitter and base regions.

Sah, Noyce, and Shockley (Ref. 4) (SNS) have shown that recombination within the emitter space charge can explain the increase of current gain with emitter current in silicon transistors.

However, Ge transistor behavior cannot be explained by space-charge recombination because in the case of a smaller energy gap one requires very short lifetimes to fit the experimental data (Ref. 5). This requirement implies a high trap density, but a uniform distribution of such traps within the emitter barrier and the base is inconsistent with the high observed gain. This leads to the requirement of traps localized within the emitter space charge.

In the present work, Ge transistor gain is changed by surface treatment, which suggests that the traps within the emitter space charge are localized at the surface. The presence of such traps in silicon transistors has been suggested recently by Sah (Ref. 6). Other recent experiments (Refs. 7, 8) have shown that the base current at low forward voltage in silicon transistors is predominantly surface current.

High-frequency, high-gain transistors are of particular interest because their design makes the usual ideal theory components of base current very small, thus emphasizing anomalous base current. That is, minority carrier injection into the emitter is minimized by heavy emitter doping. Recombination in the base is minimized by making the base width much less than a minority carrier diffusion length. At the same time the explanation of the observed $\alpha(I_E)$ based on recombination on

the base surface (Ref. 9) is excluded by the transistor geometry. That is, the base width is much less than the shortest emitter dimension, so that most of the injected carriers will diffuse and drift to the collector rather than to the surface.

It was suggested by Gummel (Ref. 10) that separate measurement of the components of dc emitter current (I_E), that is $I_B(V_{EB})$ and $I_C(V_{EB})$, would give more information than measurements of $\alpha(I_E)$. In general, if we measure small-signal current gain α,

$$\frac{\partial \log (1-\alpha)}{\partial \log I_E} = -\frac{1}{m}. \tag{1}$$

Then, when $\alpha \approx 1$,

$$\frac{\partial \log I_B}{\partial \log I_C} = 1 - \frac{1}{m}. \tag{2}$$

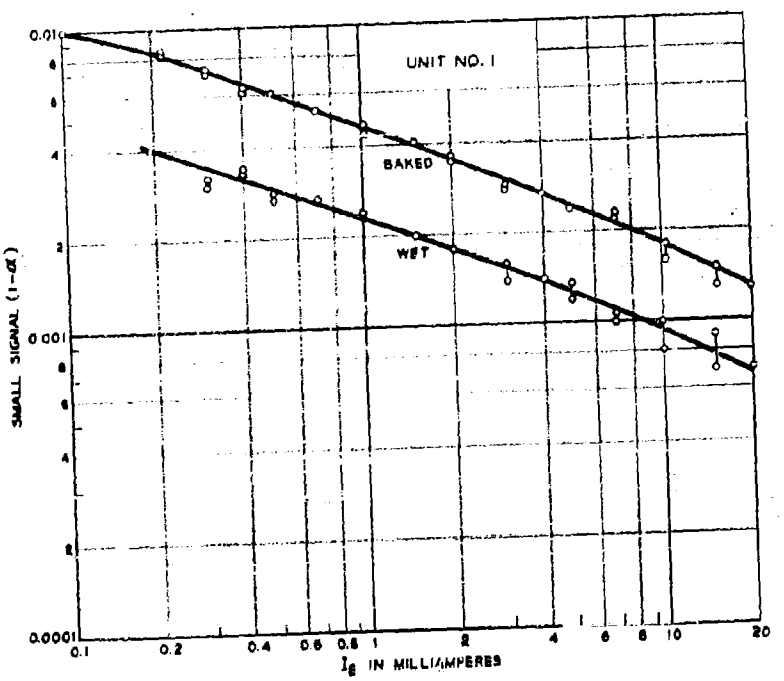

Fig. 17 - Small-signal α-defect vs. emitter current

A measurement of low-frequency ac α versus I_E in the diffused base Ge transistor shows $m \cong 3$ even up to $\alpha = 0.999$ as shown in Fig. 17. Gummel found that

$$I_C(V_{EB}) \propto e^{\frac{qV_{EB}}{kT}}, \tag{3a}$$

and

$$I_B(V_{EB}) \propto e^{\frac{qV_{EB}}{nkT}}, \tag{3b}$$

so that $\alpha(I_E)$ and $I_B(V_{EB})$ are connected by the relation between the nearly constant exponents

$$\frac{1}{m} = 1 - \frac{1}{n}. \tag{4}$$

3.2 EXPERIMENTAL

The measurements were made on transistors clamped to a constant temperature block (± 0.1° C) in a dark box flushed with dry nitrogen. Most of the measurements were made at 30°C ≡ T_R. The transistors were Ge mesa units (Refs. 11,12). Most of the measurements were made on a unit designated #1, which had a 1x6 mil alloyed Al emitter (1500-2500 Å Al), a 1 micron Sb diffused base with $C_o = 4x10^{17}$, and a 2 Ω-cm p-type collector region $2.36x10^{-4}$ cm^2 in area. Unit #2 differed in that the stripe size was 1.5x16 mil and the collector region, $10.7x10^{-4}$ cm^2 in area, consisted of 3 microns of 10 Ω-cm p-type grown epitaxially on a 0.001 Ω-cm p-type seed. A view of one of these transistors is shown in Fig. 18.

The surface cycle generally consisted of three minutes at 300°C in dry hydrogen to reach the low β state, three minutes in 60°C deionized circulating water to return to the high β state. The transistor could usually be measured for several days in either state with drifts of ≃ 10 per cent, which were small compared to the order of magnitude changes observed in changing the state of the surface. The

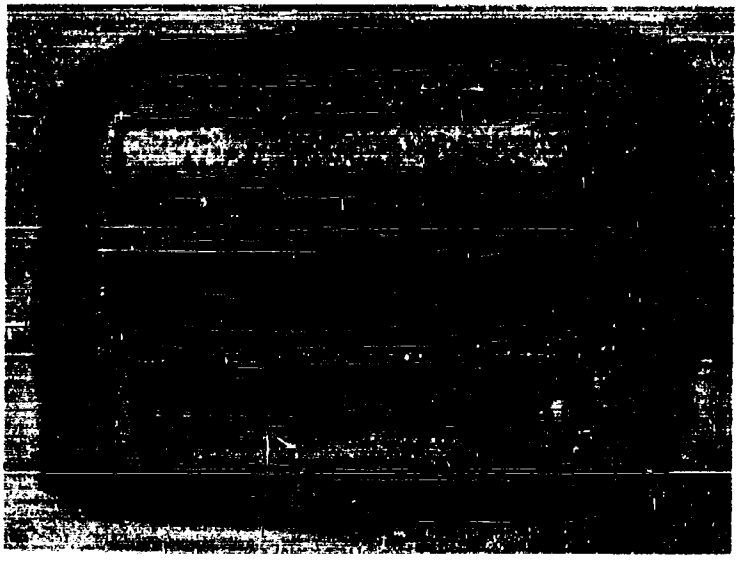

Fig. 18 - View of diffused-base germanium transistor looking down at top of mesa and showing central emitter stripe and two base stripes

treatment was not critical, that is the experimentally observed quantities could be shifted in the desired directions by adjustable amounts by longer or successive or shorter washes or bakes at various temperatures.

3.3 DISCUSSION OF THE SURFACE TREATMENT

We examine first what the surface treatment is doing to the Gc. Several cycles of base current are shown in Fig. 19. It appears that the results become more reproducible after a few cycles. We have measured the resistance between base stripes (R_{bb}) on transistors with attached leads with the result shown in Fig. 20.

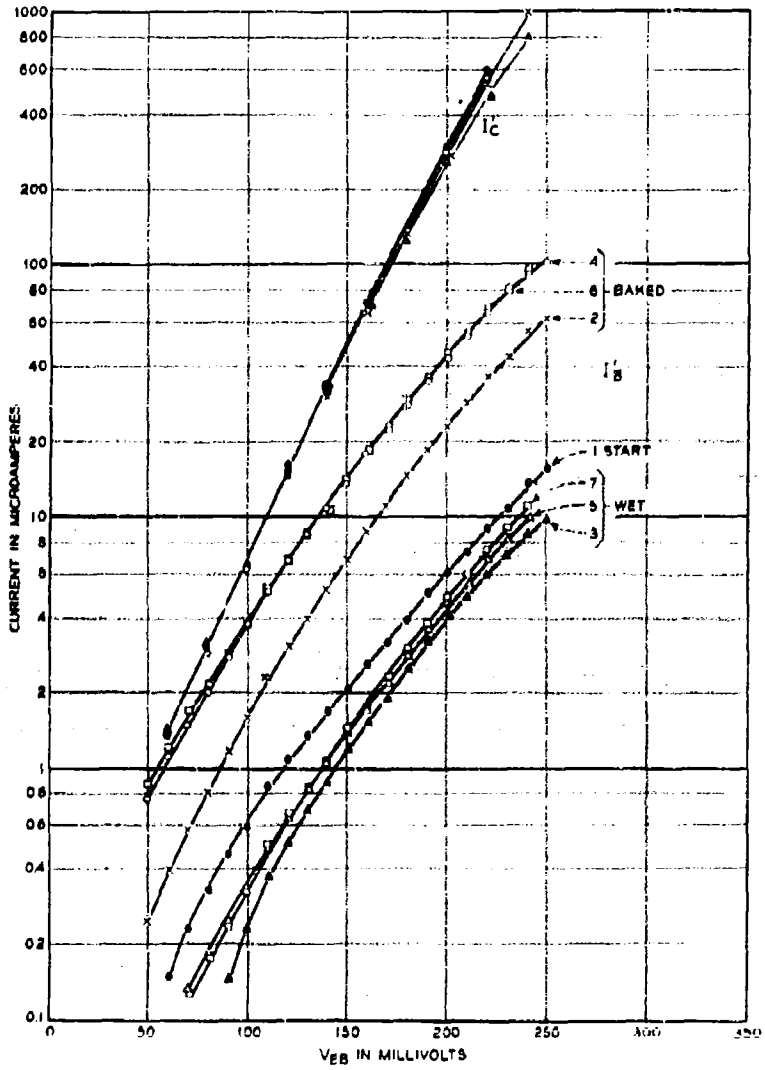

Fig. 19 - Collector and base current vs. emitter-base voltage for consecutive surface treatments

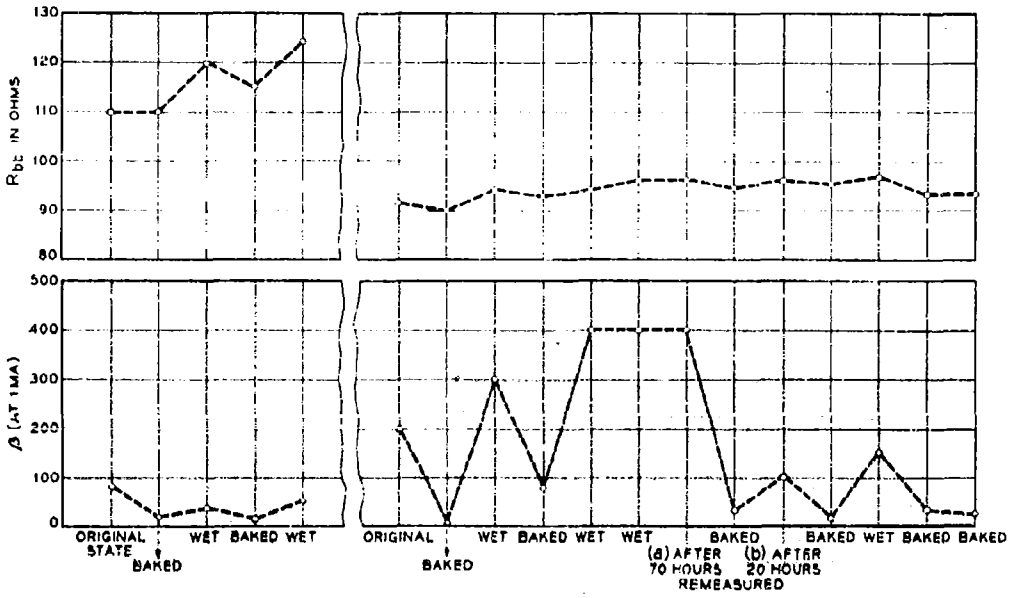

Fig. 20 - Base-base stripe transistor resistance and incremental β for consecutive surface treatments of two transistors with 1.5x16 mil stripes and 2 Ω-cm P-type collector regions (a) 70 hours at room temperature in the measuring box with dry-nitrogen flushing and (b) 20 hours at room temperature in room air about 40% relative humidity

R_{bb} is seen to increase after each water rinse and partially to recover during baking. The transistor gain is reversible in spite of the irreversible etching of the Ge.

We conclude that when we wash the unit in water containing small amounts of oxygen, we dissolve oxide, form new oxide, dissolve it, and reach a state with the unit etched slightly and covered by a "wet oxide" of reproducible thickness probably about 30 Å (Ref. 13).

In this discussion we will be interested in the density of recombination centers (N_t) at the oxide - Ge interface (Ref. 14) and in the surface charge residing mainly on and in the oxide (Refs. 14,15).

When we subject the surface to dry heat we assume that the water diffuses out (Ref. 16). We will find that the surface recombination velocity (S) increases, the surface charge becomes more positive, and that N_t increases.

We show next that dry heat increases the positive charge on the surface of our transistors. This is shown by measurements at the collector junction. We have used two transistors with the same base but with different collector regions and repeated the experiment on similar units. Unit #1 has a wide 2 Ω-cm p-type collector region. Unit #2 has a narrow 3 micron 10 Ω-cm p region followed by a p+ region. When the surface is changed from wet to baked (Fig. 21) we see no change in the differential collector capacity of unit #1. However, unit #2 in the baked state shows an increase in capacity at low reverse voltage. The increase disappears at voltages above that at which the collector space charge completely occupies the lightly doped region. From this it is deduced that an N channel (Ref. 17) is formed on the high-

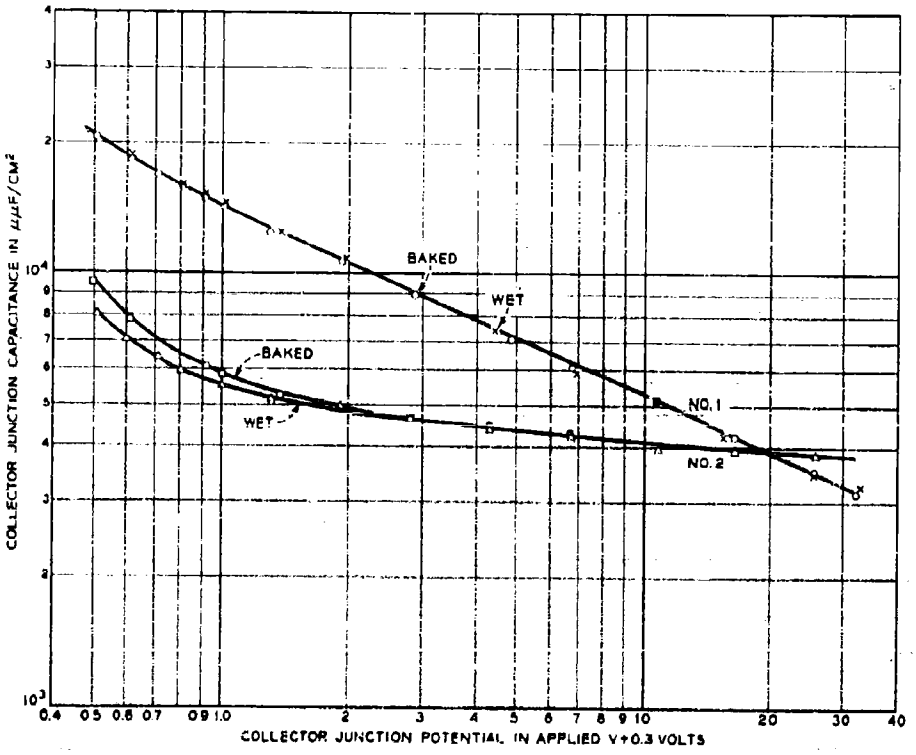

Fig. 21 - Collector capacitance vs. total junction potential for a surface cycle (No. 1 has 2Ω-cm p-type collector. No. 2 has 10Ω-cm p-epitaxial on p^+. Both have the same base diffusion)

resistivity collector region, as shown schematically in Fig. 22, but that the surface charge is not sufficient to invert 2 Ω-cm p-type.

Using the calculations of Kingston and Neustadter (Ref. 18) to obtain the surface-charge density required to invert the bulk we find in this experiment:

$$\text{on } 2\ \Omega\text{-cm p} \qquad N_s^+ < 9\text{x}10^{10}\text{cm}^{-2}$$

$$\text{on } 10\ \Omega\text{-cm p} \qquad N_s^+ > 2\text{x}10^{10}\text{cm}^{-2}\ .$$

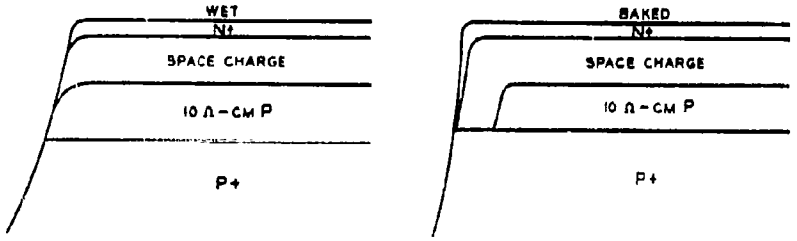

Fig. 22 - Formation of n-type channel on 10 Ω-cm p-collector region of No. 2 in the baked state

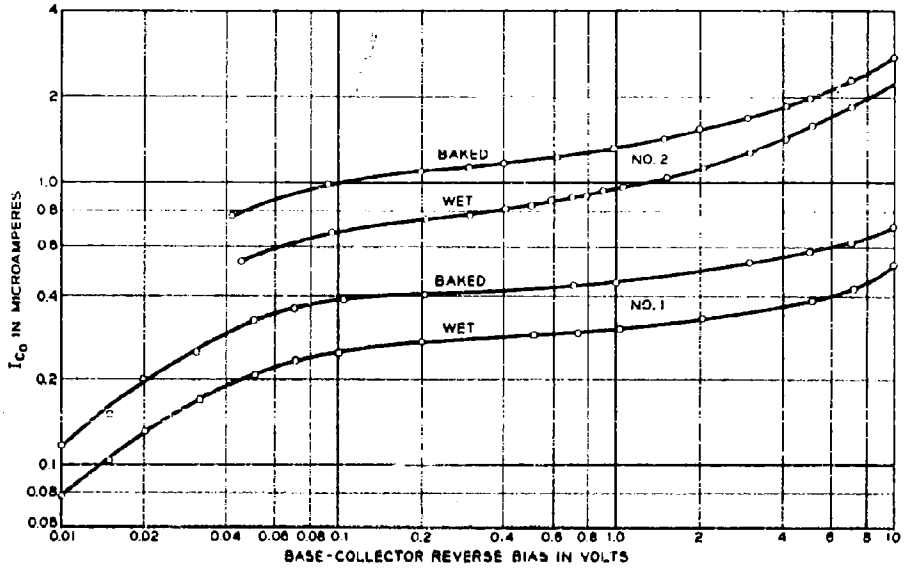

Fig. 23 - Collector junction reverse current vs. reverse base-collector voltage (emitter open)

Next we examine the collector reverse current (I_{CO}) of the two units. In Fig. 23 we see that the current has been increased at all voltages by baking whether or not a channel is present. Therefore, we conclude that baking has increased S.

There is considerable evidence that dry heating of Ge causes an increase in surface recombination velocity (Refs. 18,19,20,21). Recombination traps, or fast states, are thought to be associated with the lack of perfection at the oxide - Ge interface (Ref. 22). Law suggested that heating removed water which had an effect on the Ge oxide bond (Ref. 23). According to this point of view the number of traps is changed by heating. In addition S depends on the surface charge (Ref. 24).

We measured emitter capacity versus reverse voltage; with a Boonton Model 74-C capacitance bridge, before and after dry heat on several transistors. The results shown in Fig. 24 for unit #1 show a step junction from which the base doping at the edge of the emitter space charge is obtained (Ref. 1). A significant increase in capacity is seen in the baked state, corresponding to an increase in effective base doping at the emitter of almost 10 per cent. Such a large increase in capacity is not consistent with the heavy doping of the base at the emitter junction. The change of charge seen on the p-type collector is insufficient to account for it, if we assume the surface treatment has the same effect on all surfaces, since the charge arising from ionized surface donor states will be smaller on n-type bulk than on p-type. In the same way we cannot account for the effect of baking on R_{bb} shown in Fig. 20. To explain those results we must assume that either the surface of the base is effectively less heavily doped than the base under the emitter, or the surface charge is larger at the emitter than at the collector.

The effect of the surface treatment is summarized schematically in Fig. 25. In the discussion which follows we shall refer to the two states of the surface as the "wet" state and the "baked" state. The data were taken in several cycles and compared in pairs.

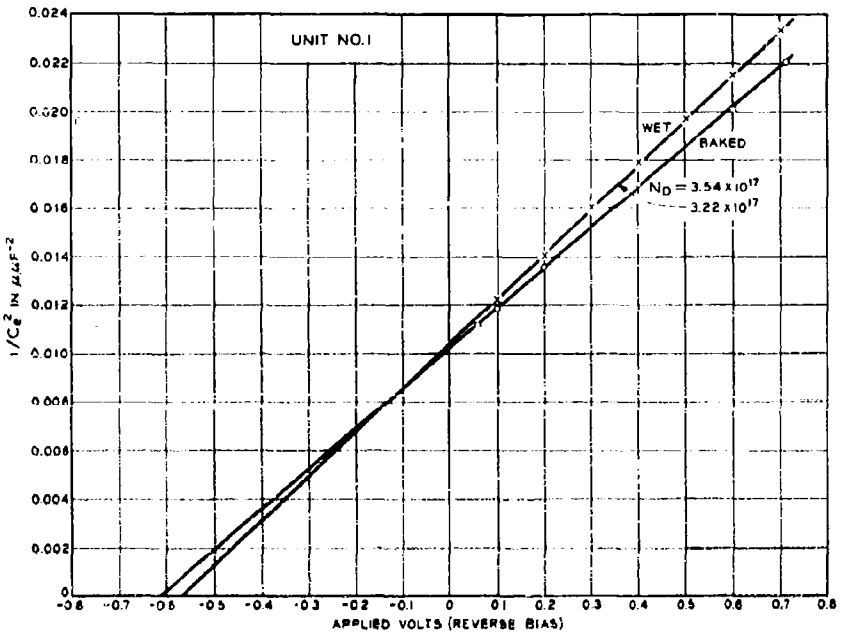

Fig. 24 - Reciprocal emitter junction capacity squared vs. reverse emitter-base voltage for transistor No. 1 in a surface cycle

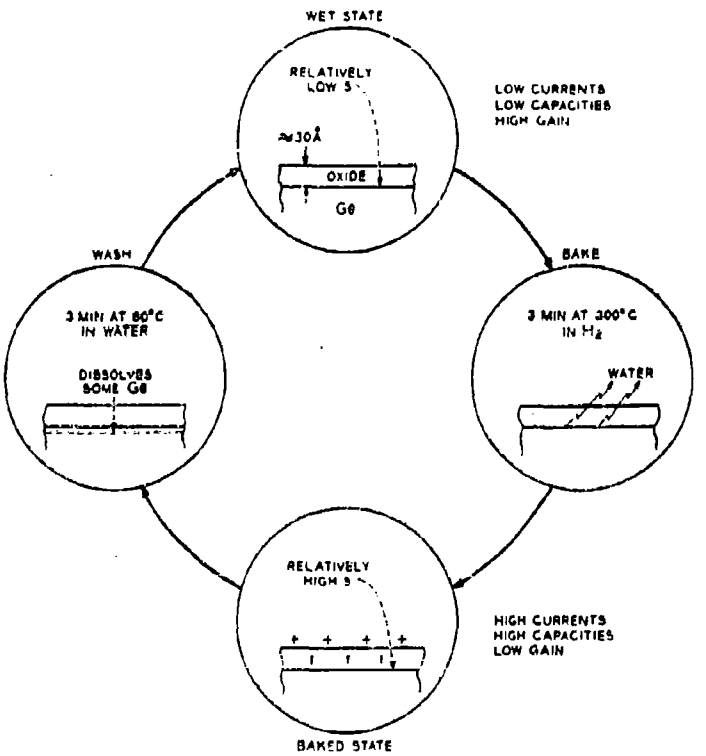

Fig. 25 - Surface treatment cycle

3.4 TRANSISTOR CURRENTS AS A FUNCTION OF V_{EB}

DC base and collector currents, with the transistor at constant temperature, were measured in the circuit shown in Fig. 26. The circuit noise is equivalent to 2 μv across 1000 ohms at the input to the dc amplifier, which allows us to measure currents as small at 0.02 μa. With $V_{EB} = 0$, the base current flowing into the base due to the reverse bias on the collector was balanced out. Then the current flowing out of the base due to forward emitter bias,

$$I_B' = I_B(V_{EB}) - I_B(0), \tag{5}$$

was obtained as shown by the data points in Fig. 27 for transistor #1, for two states of the surface. The same data may be obtained by holding $V_{CB} \cong 0$, in which case $I_B(0) = 0$. $I_B(-V_{EB})$ does not saturate as ideal pn junction theory (Ref. 25) would predict, so $V_{EB} = 0$ is the only voltage at which we may balance to obtain I_B'. However, $I_C(V_{EB})$ obeys theory and we may balance I_C at V_{EB} a few tenths volt negative, to obtain data convenient for plotting near $V_{EB} = 0$.

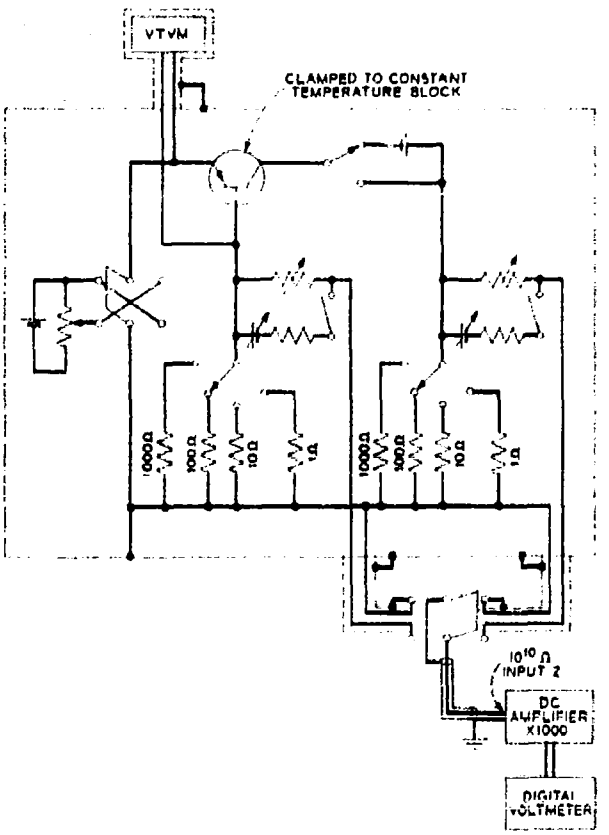

Fig. 26 -- Transistor dc measuring circuit

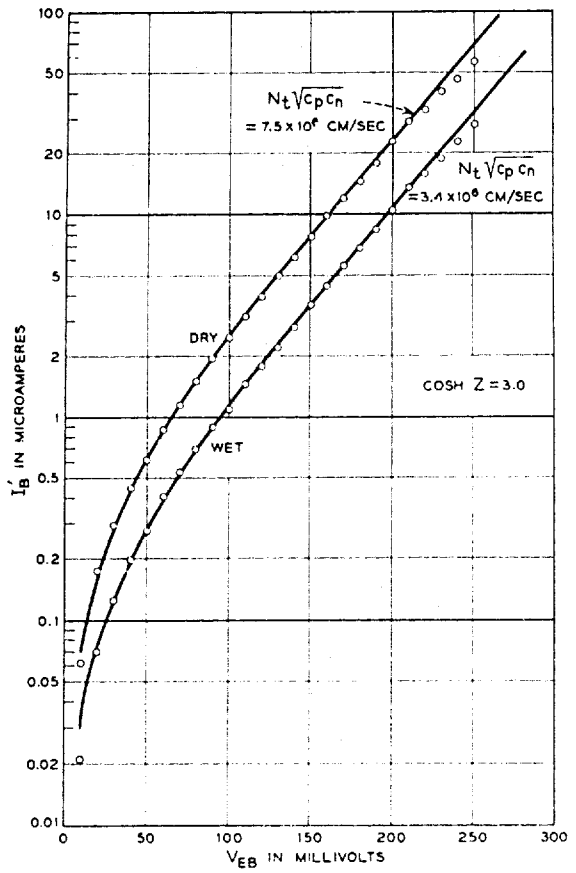

Fig. 27 - Base current vs. emitter-base voltage for transistor No. 1 in different states
Solid curves are Equation (17)

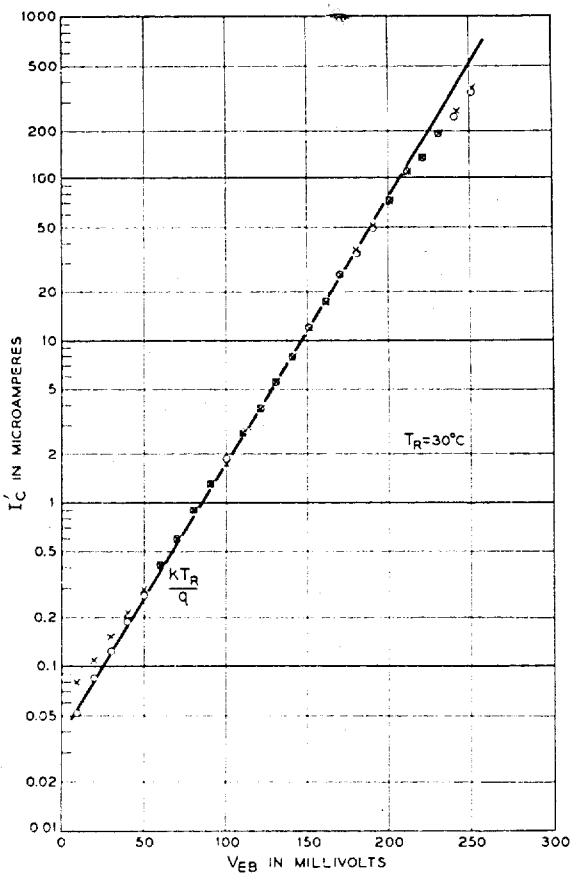

Fig. 28 - Collector current vs. emitter-base voltage measured at the same time as data of Fig. 27
Solid line is kT_R/q. The low voltage deviations are attributed to inaccuracy in balancing out I_{CO}

$$I'_C = I_C(V_{EB}) - I_C(-0.2v) \tag{6}$$

is plotted in Fig. 28.

For 100 mv $< V_{EB} <$ 200 mv,

$$I'_C = I'_{C_1} \exp \frac{qV_{EB}}{kT}$$

$$T = 30°C \tag{7}$$

$$I'_B = I'_{B_1} \exp \frac{qV_{EB}}{nkT}$$

It can be seen that I'_C is virtually unaffected by surface change whereas I'_B increases in the baked state, being displaced parallel to itself.

At high forward voltage the currents deviate from simple exponentials due to series resistance from the point contacts which causes the measured applied voltage to be greater than the internal V_{EB}. The relation between the two currents can be shown to continue to higher voltage by measuring 1 - α, which involves the ratio of the currents. This is shown in Fig. 17, where small signal 1 - α is plotted versus I_E and the slope is nearly constant.

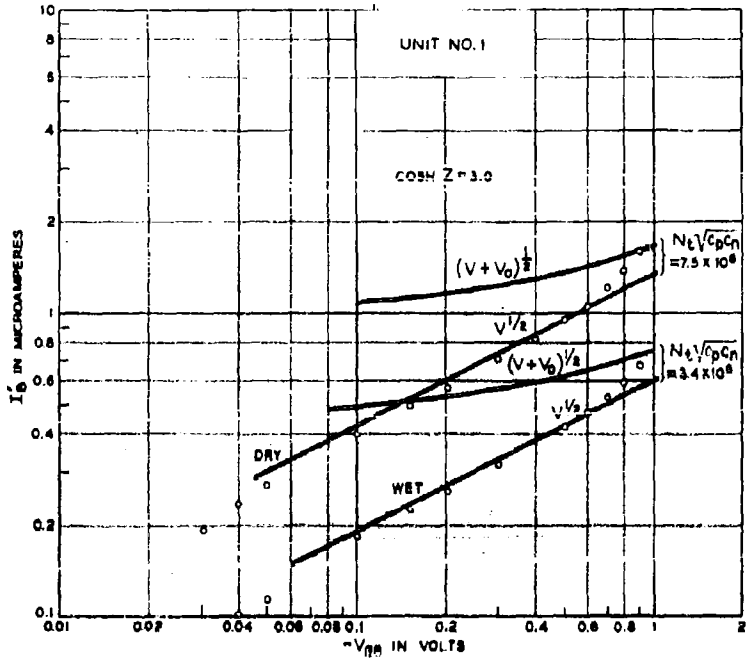

Fig. 20 - Base current vs. reverse emitter-base voltage with collector reverse biased, measured in the same cycle as data of Fig. 27
Solid lines are Equation (15) with V_{OS} = 570 mv
(obtained from Fig. 24) and V_{OS} = 0

The base current I'_B for V_{EB} negative is shown in Fig. 29. Although $I'_C(-V_{EB})$ saturates, $I'_B(-V_{EB})$ does not saturate and is surface dependent. These reverse currents were measured at the same time as the forward currents shown in Fig. 27. Comparing the base currents, we find that in the surface cycle forward and reverse currents have been shifted in the same ratio.

We see, therefore, that ideal pn junction theory seems to apply to the collector current, but not to the base current. The base current, calculated from the theory of diffusion and recombination in the bulk, gives $I'_B \propto \exp \frac{qV_{EB}}{kT}$ which is not observed anywhere in the entire operating range of the transistor. We conclude that the bulk base current in these Ge transistors is small, compared to the surface dependent base current.

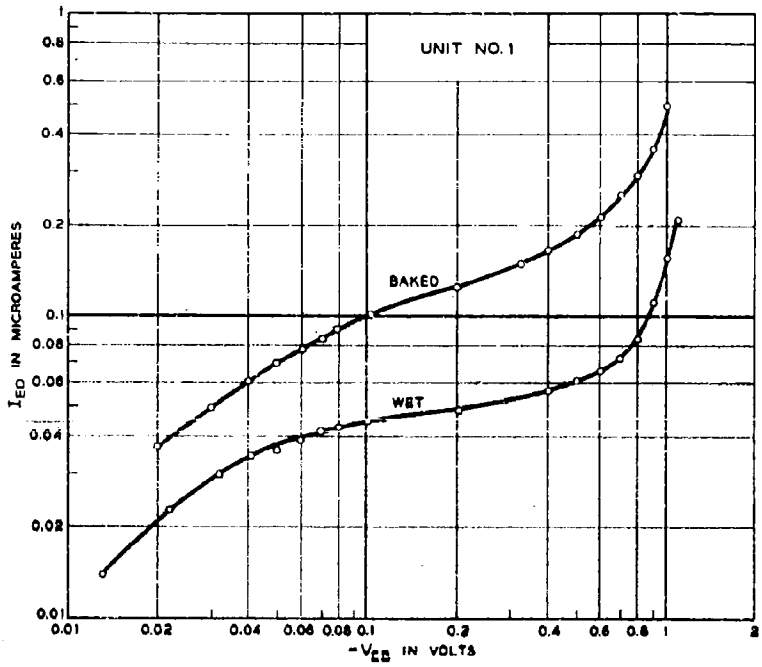

Fig. 30 - Base current vs. reverse emitter-base voltage with collector open, for a surface cycle

The saturation value of I'_B is given by ideal pn junction theory (Ref. 25).

$$I'_B(-V_{EB}) = \frac{1 - \alpha_N}{1 - \alpha_I \beta_N} I_{Eo} \qquad (8)$$

where I_{Eo} is the reverse emitter-base diode current with collector open. I_{Eo} in both surface states is shown in Fig. 30. Here, one sees a saturation current added to the surface dependent current. From a comparison of Figs. 30 and 29, we conclude that $\alpha_N \tilde{=} 1$ even at very low current.

3.5 MODEL OF THE BASE CURRENT

We have found that the base current is surface dependent and has a dependence on emitter-base voltage similar to that calculated for space-charge recombination due to deep-lying traps (Ref. 4). As previously noted, volume space-charge recombination is inconsistent with high attainable current gains such as those shown in Fig. 17.

We will, therefore, assume that the surface dependent base current arises from recombination or generation at deep-lying traps, which are localized at the oxide-Ge interface within the emitter space-charge.

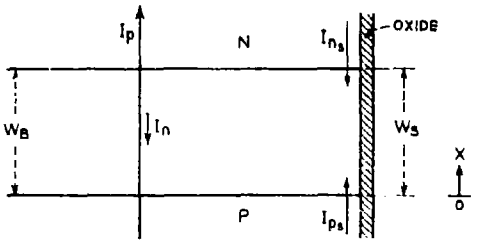

Fig. 31 - Schematic representation of current flow under forward bias in the emitter-base space-charge region near the surface. $W_S = W_B$ case

Consider the currents flowing across the p^+n emitter junction under forward bias as shown in Fig. 31. Near the surface, the hole current (I_{p_s}) is in part recombined in transit across the space charge and an electron current, (I_{ns}) flows in from the base equal to the hole recombination current. Away from the surface the hole current, (I_p), flows across to the collector without significant recombination loss and the electron current (I_n) is very small because the transistor has been designed to give an emitter efficiency within the bulk of approximately unity.

The current resulting from recombination of holes and electrons via surface traps may be thought of as flowing into the surface. The current density is

$$j(x) = qU(x), \tag{9}$$

where U(x) is the surface recombination rate per cm^2 at the position (x) along the space-charge surface. The surface current is then

$$I_S = L \int_0^{W_S} j(x)dx, \tag{10}$$

where L = junction perimeter and W_S = junction width at the surface.

The surface recombination rate for the non-degenerate case is given by (Refs. 26,4,24)

$$U(x) = \frac{n_1 \; N_t \sqrt{c_p c_n} \; \sinh \dfrac{q\left(\varphi_{p_s} - \varphi_{n_s}\right)}{2kT}}{\cosh\left[\dfrac{q}{kT}\left(\psi_S(x) - \dfrac{\varphi_{p_s} + \varphi_{n_s}}{2}\right) + \dfrac{1}{2}\ln\dfrac{c_n}{c_p}\right] + e^{-\frac{q\left(\varphi_{p_s} - \varphi_{n_s}\right)}{2kT}} \cosh\left[\dfrac{E_t - E_i}{kT} + \dfrac{1}{2}\ln\dfrac{c_n}{c_p}\right]}$$

assuming a single trap energy E_t. $N_t c_n$, (Ref. 19) is defined as the surface recombination velocity in a highly p-type surface, $N_t c_p$ in a highly N-type and the notation is the same as that of SNS where $\psi_s(x) = -\frac{E_{i_s}}{q}$ is the electrostatic potential and φ_{p_s} and φ_{n_s} are the quasi-Fermi potentials all at the surface.

Surface recombination velocity may be defined as:

$$S = N_t \sigma v \tag{12}$$

so that

$$\frac{c_n}{c_p} = \frac{\sigma_{no}}{\sigma_{po}} \tag{13}$$

and

$$N_t v \sqrt{\sigma_{no}\,\sigma_{po}} \quad \alpha \quad N_t \sqrt{c_p c_n} \tag{14}$$

where σ_{no} is the cross section for electron capture in a highly p-type surface, v is thermal velocity for electrons and holes, and N_t is the density of surface recombination centers per unit area.

Under reverse bias U changes sign and expresses the generation rate of electrons or holes at the position x. $\varphi_n > \varphi_p$ within the space charge and at moderate reverse bias the generation rate becomes independent of voltage and position. Then,

$$I_g(V < 0) = I_R = \frac{qLW_S n_i N_t \sqrt{c_p c_n}}{2\cosh\left[\frac{E_t - E_i}{kT} + \frac{1}{2}\ln\frac{c_n}{c_p}\right]}, \quad \frac{-qV}{kT} \gg 1 \tag{15}$$

will depend on the reverse voltage through

$$W_S = \left[\frac{2K\epsilon_0(V_{os}-V)}{qN_S}\right]^{1/2} \tag{16}$$

in the case of a step junction, where $V = V_{EB}$, V_{os} is the junction contact potential at the surface, N_S is the charge per unit volume at the surface of the base and $K\epsilon_0$ and q have the usual meaning.

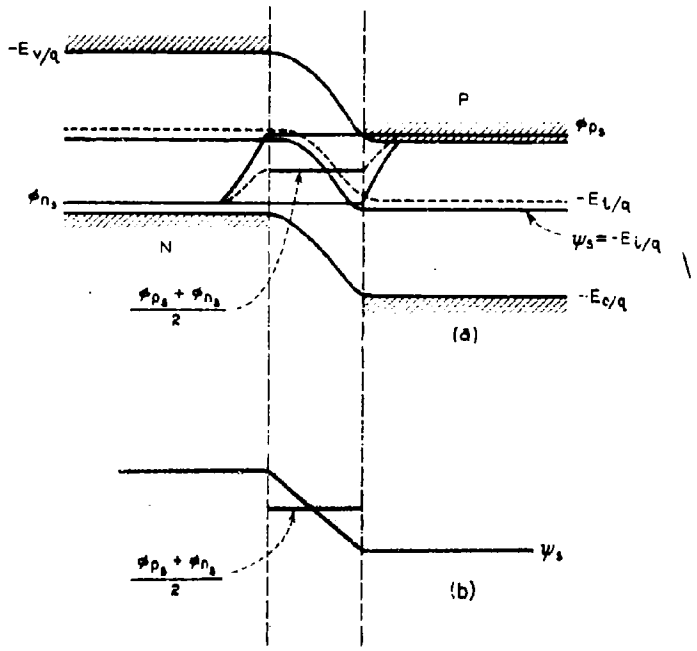

Fig. 32 - (a) Potentials at the surface in a p^+n junction like an alloyed Al emitter on an n-type base
(b) Linear potential approximation

Under forward bias the integration of Equation (10) requires a detailed knowledge of the spatial dependence of the potential and of the carrier concentrations at the surface. We will do the integration to obtain the surface current using the same approximate method described by SNS for the volume recombination current. The reader is referred to their paper for more detailed discussion than that presented here. In Fig. 32(a) is shown a potential diagram of a p^+n step junction which is like that expected for an alloyed Al emitter junction. The imrefs have been shown to be approximately straight across the space charge (Ref. 4). In Fig. 32(b) is the approximation to the potential made to simplify the integration to the SNS form. The potential is assumed to vary linearly with distance across the space charge, and the crossover at which electron and hole concentrations are equal is taken at the center of the space charge.

With these simplifying assumptions the integration gives

$$I_s(V > 0) = I_B = \frac{qLW_S n_i N_t \sqrt{c_p c_n}\ 2 \sinh \frac{qV}{2kT}}{(V_{os} - V)\ \frac{q}{kT}} f(b) \qquad (17)$$

$$= B\, f(b)\, \frac{\sinh \frac{qV}{2kT}}{(V_{os} - V)^{1/2}}$$

where

$$B = 2kT\, n_i L \left(\frac{2K\epsilon_o}{qN_s}\right)^{1/2} N_t \sqrt{c_n c_p}$$

$$b = e^{-\frac{V}{2kT}} \cosh\left[\frac{E_t - E_i}{kT} + \frac{1}{2} \ln \frac{c_n}{c_p}\right] = e^{-\frac{V}{2kT}} \cosh Z$$

and f(b) (Ref. 4) is plotted in Fig. 33. As SNS have shown

$$I_B \sim e^{\frac{qV}{nkT}} \tag{18}$$

where $1 < n < 2$, approaching unity as the quantity $E_t - E_i/kT + \frac{1}{2} \ln \frac{c_n}{c_p}$ becomes large of order 10.

Two conclusions may be drawn at once from the model.

1. The observed base current may be fitted.

2. The fact that the base current is observed to shift parallel to itself in the surface cycle says that it is the trap density that is being changed rather than the type of trap.

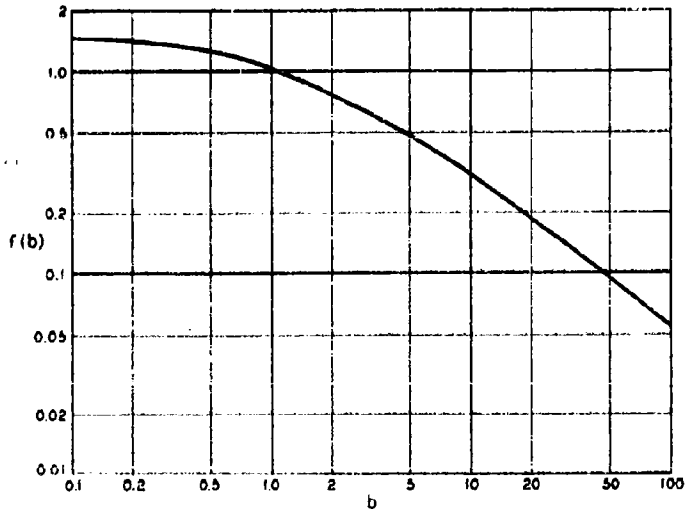

Fig. 33 - The function f(b)

3.6 COMPARISON OF EXPERIMENT WITH THEORY

In Fig. 27 the solid lines are the forward base current I_B given by Equation (17) where the fit has been chosen at V_{EB} = 60 mv and 150 mv. The fit to the experimental data determines the magnitude of the constants B and Z in Equation (17). For both curves for this transistor

$$\cosh Z = 3.0. \tag{19}$$

In order to estimate the surface recombination velocity factor, $N_t \sqrt{c_p c_n}$, we will assume that L is the perimeter of the 1 x 6 mil emitter, L = 3.56×10^{-2} cm, and $N_S = N_B$, the average base doping within the emitter-barrier volume, which from Fig. 24 is approximately 3.2×10^{17} cm^{-3}. Using

n_i = 2.5×10^{13} cm^{-3}

K = 16

ϵ_o = 8.85×10^{-14} farads/cm

q = 1.6×10^{-19} coulombs

$\frac{kT_R}{q}$ = 0.026 volts

we obtain

$N_t \sqrt{c_p c_n}$ ("wet" state) = 3.4×10^6 cm/sec

$N_t \sqrt{c_p c_n}$ ("baked" state) = 7.5×10^6 cm/sec.

We examine this result in the discussion section.

According to the theory the same two parameters for each state uniquely determine the reverse current arising from space-charge generation at $-V_{EB} >> \frac{kT}{q}$. The solid lines in Fig. 29 have been calculated from Equation (15) using the above parameters, and agreement is found from 0.1 to 0.6 volt, with the current proportional to $V^{1/2}$ not $(V+V_{os})^{1/2}$.

This result is unexpected. Channel theory (Ref. 27) does not predict a slope as large as $V^{1/2}$. Diffusion current would tend to saturate and can be shown to give a negligible contribution. A shunt resistance gives a V^1 slope and is easily recognized as a hump in the forward direction at low currents. Furthermore, the magnitude of the current as well as the slope is given by $V^{1/2}$. The currents are well above the noise in this measurement. A $V^{1/2}$ slope of $I'_B(-V_{EB})$ is obtained independent of reverse collector bias. It is seen repeatedly on different units and over a range of temperature (Fig. 38). Above 0.6 volt, multiplication dominates in these heavily doped junctions which accounts for the deviation of the experimental current above the $V^{1/2}$ slope.

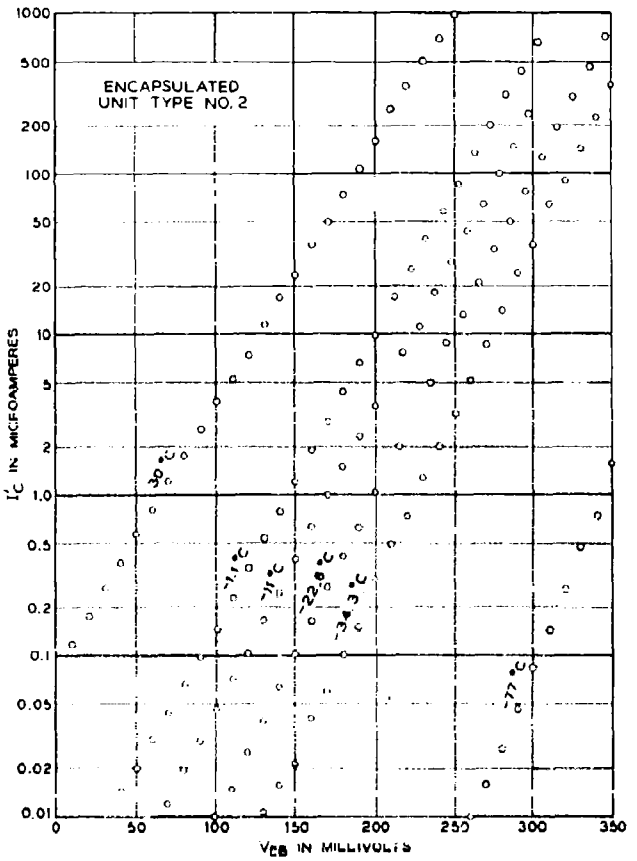

Fig. 34 - Collector current vs. emitter-base voltage and temperature for a vacuum encapsulated transistor of type No. 2

Under reverse bias the generation rate and therefore the current does not depend on the surface potential. Therefore, the shift in the current when the state of the surface is changed must be due to a shift in the surface recombination velocity parameter. Taking into consideration the fact that the slope of the current under forward bias does not change in the shift (cosh Z = const.) we conclude that only the number of fast states, N_t, changes.

We show next that the theory predicts the temperature dependence of the forward base current. For this experiment we used a vacuum encapsulated unit similar to unit #2. This sealed unit was used so it could conveniently be immersed in a cooling bath. In Figs. 34 and 35 are shown the I'_C and I'_B current data. We see that, as the temperature is lowered, I'_C becomes smaller than I'_B a result contrary to ideal PN junction theory. At the lower temperatures

$$n(T) = \text{const.} = 1.55 \pm .01 \quad .$$

At moderately large forward voltage we can write Equation (17) in the form

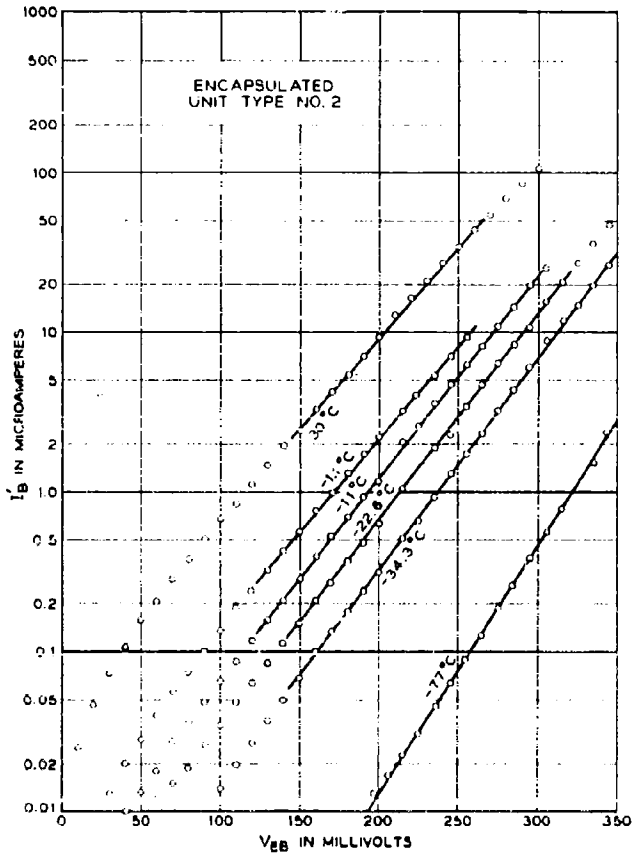

Fig. 35 - Base current vs. emitter-base voltage and temperature measured at the same time as the data of Fig. 34

$$I_B = \frac{2qLW_B n_i}{(V_{OS}-V)^{1/2}} \; N_t \sqrt{c_p c_n}\, \frac{kT}{q} \; e^{\frac{qV}{nkT}} . \qquad (21)$$

Also

$$N_t \sqrt{c_p c_n} \propto N_t v \sqrt{\sigma_{no}\sigma_{po}} \propto T^{1/2}, \qquad (22)$$

assuming that the temperature enters only in $v \propto T^{1/2}$. Then

$$I_B = \text{Const.}\; T^3 e^{-\frac{Eg_o}{2kT} + \frac{qV}{nkT}} \qquad (23)$$

and

$$E_{act} = - \frac{k}{\log e} \frac{\partial \log \frac{I_B}{T^3}}{\partial \frac{1}{T}} = \frac{Eg_o}{2} - \frac{qV_{EB}}{n} \quad . \tag{24}$$

From the data shown in Fig. 35, we plot $\log \frac{I'_B}{T^3}$ versus $\frac{1}{T}$ in Fig. 36 at two voltages and obtain

$$Eg_o = 2\left[E_{act} + \frac{qV_{EB}}{n}\right] = \begin{matrix} 0.766 \text{ ev} & (V_{EB} = 200 \text{ mv}) \\ 0.778 \text{ ev} & (V_{EB} = 250 \text{ mv}) \end{matrix} \tag{25}$$

in good agreement with $Eg_o = 0.785$ ev (Ref. 28). In the same way it can be shown that the collector current, unlike the base current, has a temperature dependence given by ideal pn junction theory.

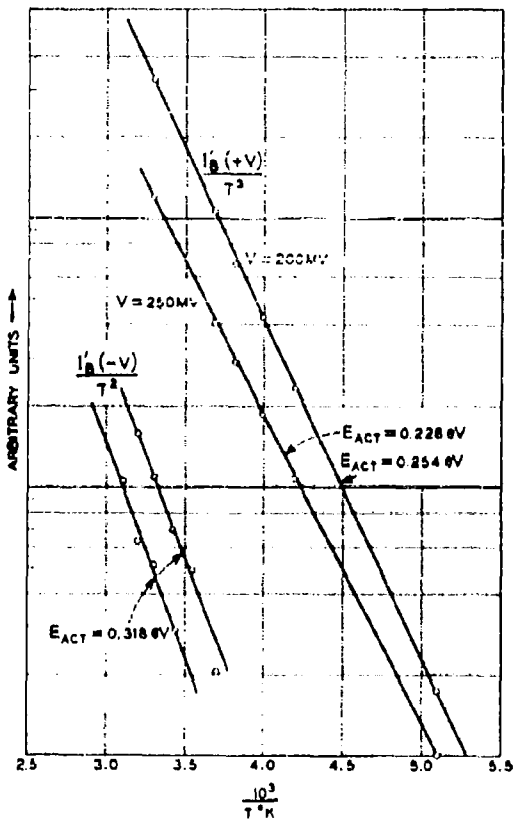

Fig. 36 - Temperature dependence of base current under forward and reverse bias
(The upper points are 200 mv and 250 mv data from Fig. 35. The lower points are from the $V^{1/2}$ portion of the curves of Figs. 37 & 38)

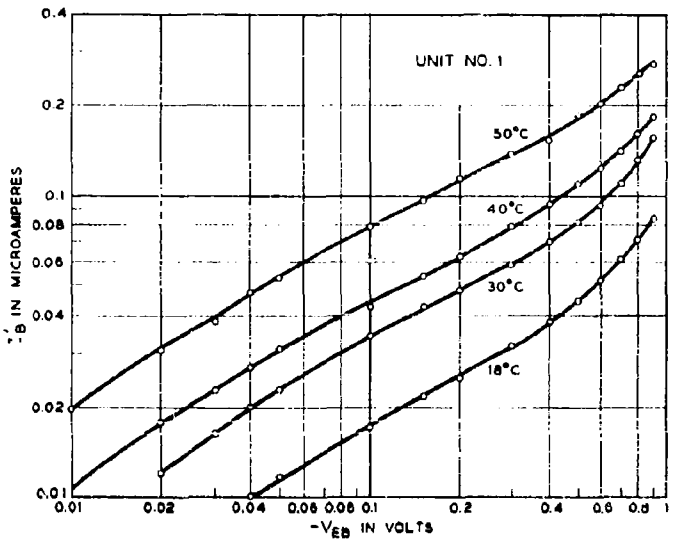

Fig. 37 - Base current of open unit No. 1 vs. reverse emitter-base voltage at various temperatures. Collector reverse biased

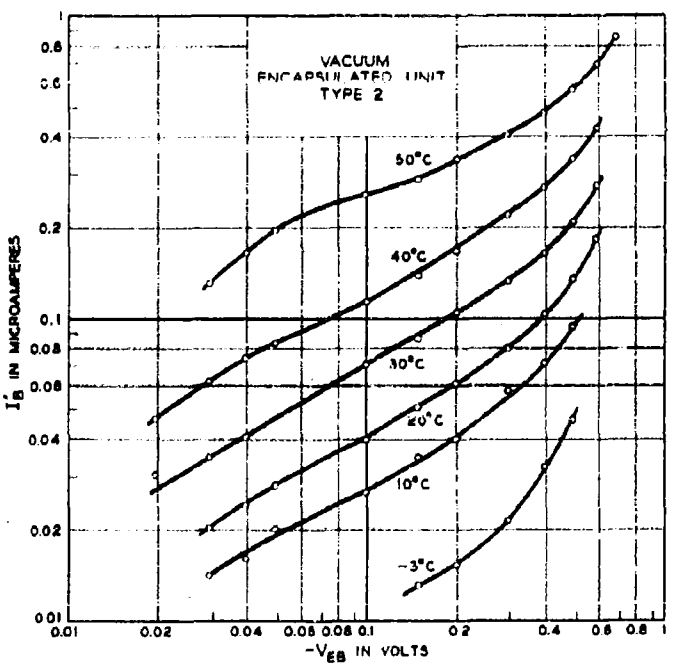

Fig. 38 - Base current of vacuum encapsulated unit type No. 2 vs. reverse emitter-base voltage at various temperatures. Collector reverse biased

The temperature dependence of the reverse current may be used to obtain the energy of the recombination generation centers. (Ref. 4). These data were obtained on unit #1 as shown in Fig. 37. Similar data (Fig. 38) were taken on a vacuum encapsulated unit of the same type as #2. The two units give nearly the same activation energy even though one is open and the other has been vacuum baked and sealed. Equation (15) gives, for the activation energy,

$$E_{act} = -\frac{k}{\log e}\,\frac{\partial \log\left(\frac{I_B}{T^2}\right)}{\partial \frac{1}{T}} = \frac{Eg_o}{2} + (E_t - E_i)\tanh Z, \qquad (26)$$

where $\tanh Z \tilde{=} \pm 1$ (Appendix I). From the data plotted in Fig. 36 we obtain

$$E_t - E_i = \bar{+}\,80 \text{ mv} \qquad (27)$$

which is similar to values previously reported for surface recombination centers in Ge (Refs. 29,30,31). Equations (19,26 and 27) then give (Appendix I)

$$\left(\frac{c_n}{c_p}\right)^{\pm 1} = 1.5\times10^{4}\,. \qquad (28)$$

Such large c_p/c_n have been reported in the literature (Ref. 29).

To summarize, we have found that the base current with forward and reverse emitter-base voltage is entirely surface current at and below room temperature in the heavily doped emitter-base configuration of these Ge transistors. We have found quantitative agreement with the theoretical voltage and temperature dependence of the forward base current and have shown that $I_B^{\downarrow}(+V_{EB})$ and $I_B^{\downarrow}(-V_{EB})$ were related as predicted by the surface model.

However, we have found that $I_B^{\downarrow}(-V_{EB})$ increases as $V^{1/2}$ which the model does not predict. Also, with the assumption that the junction width at the surface is the same as in the bulk, we have obtained larger values of the surface recombination velocity factor, $N_t\ \sqrt{c_p c_n}$.

3.7 MODIFIED MODEL

The two points of disagreement between theory and experiment suggest that the surface of the transistor in the vicinity of the emitter junction is effectively lightly doped so that the space charge is wider at the surface than within the bulk and the contact potential, $V_{os} \gtrsim 50$ mv under reverse bias.

It will be assumed that when a fresh oxide is formed in the fringing electric field of the junction, a charge configuration forms on the oxide (Refs. 32, 33) in such

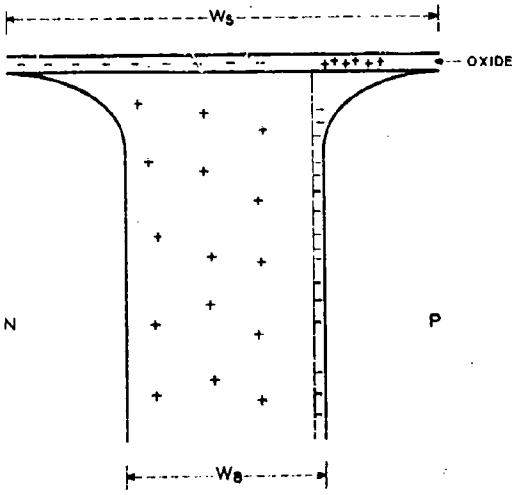

Fig. 39 - Model of emitter barrier at the surface, both edges depleted such that $W_S > W_B$ and $V_O \rightarrow 0$

a way as to screen the electric field near the surface (Fig. 39). The junction at the surface with no applied bias is then like that between p and n regions both lightly doped.

Under reverse bias, the junction at the surface widens mainly into the base side giving a $(V+V_{OS})^{1/2}$ surface current dependence with $V_{OS} \ll V$. Under forward bias the junction at the surface narrows rapidly at first then more slowly as the array of screening charge is left behind and decays. The forward base current is not sensitive to this $(V_{OS}-V)$ voltage dependence because of the presence of factors exponential with voltage.

As evidence of this depletion at the surface junction edges we note the large change in emitter junction capacitance which occurs when the surface charge is changed (Fig. 24) which, as discussed previously, appears inconsistent with a heavily doped base surface.

3.8 DISCUSSION

The results presented here on Ge mesa transistors are believed to apply with considerable generality to Ge high frequency high gain transistors which differ in details of geometry, doping, etching, and encapsulation, because $n \cong 1.5$ is generally observed on these transistors, as shown in Table 3-1.

The traps which are seen may be characteristic of an ordinary oxidized Ge surface. Since a range of different surface treatments has relatively little effect on $\alpha(I_E)$, it would seem that the traps are associated with the Ge-oxide bond structure. The role of water may be to deactivate the trap by shifting its energy out of the Ge energy gap (Ref. 16).

The increase of interface traps, or fast states, on Ge after elevated temperature treatment has been attributed to oxidation (Ref. 32). Heating before field effect stud-

Table 3-1

COMPARISON OF A SMALL SAMPLE OF GERMANIUM TRANSISTOR TYPES

Germanium Type	Cutoff* Frequency	Gain = $\frac{\Delta I_C}{\Delta I_B}$†	n
pnp Diffused Base	500 mc	150	1.5
pnp Microalloyed	150	100	1.4
pnp Post Alloy-Diffused	340	100	1.3
npn Mesa	250	80	1.6
npn Mesa	470	160	1.6

*From extrapolation of 100 mc gain measurement at I_E = 1 ma.

†At I_C = 1 ma.

ies of Ge is usually done in air (Ref. 20,21) or oxygen (Ref. 16). The surface recombination velocity is found to increase (Refs. 16,20) and the surface found to be n-type (Ref. 16). However, heating in vacuum also increases S (Refs. 19,34).

In the present experiments heating is done in deoxygenated hydrogen. We know that oxidation is not occurring to an appreciable extent during heating because the change in sheet resistance of a thin layer is nearly the same for a wash-bake-wash cycle as for a wash-wash cycle as seen in Fig. 20. We conclude that it is the baking accompanied by water removal rather than oxidation which increases fast state density.

The values of $N_t \sqrt{c_p c_n}$ which are estimated from the fit of theory with experiment are in the 10^6 - 10^7 cm/sec. range for the currents in Fig. 27. They may be compared with values of 10^4 - 10^5 cm/sec. obtained from field effect on high-resistivity Ge (Refs. 34,35). Although the present values are for a particular case, we encounter similar results with other transistors. We have already pointed out that our assumed value of space-charge width at the surface (W_s) is probably too small. In addition we have taken the perimeter of the space charge (L) to be the nominal dimensions of the emitter. This may be too small also, if the emitter regrowth edge is "wrinkled" appreciably. Thus, we may have overestimated $S \propto (LW_s)^{-1}$. However, the large values of surface recombination velocity may have some validity because of the fact that the emitter junction is between very heavily doped regions and only a few hundred angstroms from an Al-Ge eutectic region.

Equation (17) was obtained by using the recombination rate expression for a single trap and assuming that the potential at the surface is such that the maximum of the recombination rate occurs midway across the space charge. These assumptions give a dependence of forward base current on voltage and temperature which

is in agreement with experiment. Also, at moderate reverse bias, the assumption concerning $\psi_s(x)$ is not involved in the calculation of the reverse current and we find that the magnitude of the reverse current is given by the constant $\frac{B}{\cosh Z}$ obtained from the forward current.

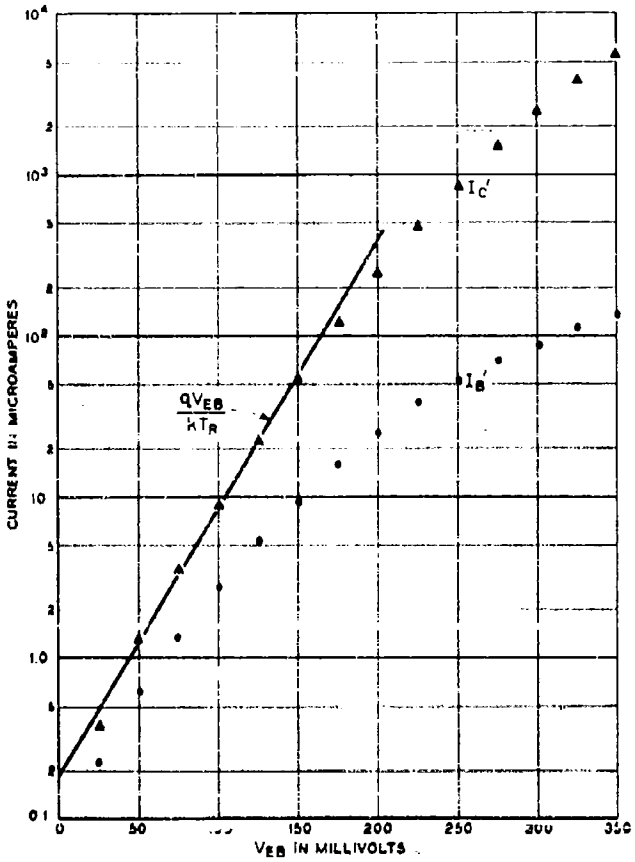

Fig. 40 - Current vs. emitter-base voltage for an out-diffused transistor of type No. 1

In Fig. 40 are shown the current voltage curves for a transistor similar to unit #1 except that the surface concentration of the base has been depleted by out-diffusion. This was first observed by Gummel. The shape of the I_B curve is interpreted as being due to a large decrease in emitter space charge width with increased forward bias resulting from the lower donor concentration near the surface.

Certain calculations are changed by the preceding results. In these transistors current gain, α, cannot be obtained from emitter efficiency, γ, calculated from doping. The Ebers-Moll relations between currents do not apply. Base resistance at low frequencies must be calculated for base current flow primarily into the emitter edges.

3.9 SUMMARY

The base current in high-frequency germanium diffused-base transistors has a dependence on emitter-base voltage and on temperature which is shown to be in quantitative agreement with the theory of recombination at traps within the emitter space charge, with energy near the mid-gap. However, as pointed out by Moll, the trap density required in this model is so high that a homogeneous distribution of such traps in the base region near the emitter barrier is inconsistent with the high gain observed.

The base current is also found to be strongly surface dependent. Common emitter current gain can be cycled repeatedly such that it changes by factors of order ten. Washing in water is used to decrease base current, baking in dry hydrogen to increase it. The base current under reverse emitter-base voltage shows quantitatively the same surface dependence as that seen under forward bias.

These results suggest that base current in these transistors is dominated by recombination at surface traps within the emitter space charge. A contribution to the base current in silicon transistors arising in a similar way has been suggested by Sah.

The data suggest that the emitter at the surface at equilibrium, has a configuration like a junction between p and n regions both lightly doped and that surface recombination velocity is high.

The single-trap approximation gives a trap 80 mv from the mid-gap. The traps are thought to be characteristic of the Ge-Ge oxide interface and to be deactivated by the presence of water.

When a transistor which has been washed in water is later baked in hydrogen, the same trap persists, its density increases, and the surface positive charge also increases.

Collector current depends on emitter-base voltage and temperature as expected from ideal pn junction theory and is nearly independent of surface treatment. The different dependence of base and collector current on emitter-base voltage results in the well-known dependence of common emitter current gain on current. The model is believed to apply to germanium high-frequency, high-gain transistors which show $I_B \tilde{\alpha} \exp\left(\frac{qV_{EB}}{1.5kT}\right)$ which included virtually all currently available types with diffused base layers.

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APPENDIX I

From Equations (15) and (22),

$$I_R(T) = \text{Const } T^2 \frac{e^{-\frac{Eg_o}{2kT}}}{\cosh Z(T)},$$

where

$$Z = \frac{E_t - E_i}{kT} + \frac{1}{2} \ln \frac{c_n}{c_p} .$$

$$\ln \left(\frac{I_R}{T^2} \right) = - \frac{Eg_o}{2kT} - \ln \cosh Z$$

$$E_{act} = -k \frac{\partial \ln \left(\frac{I_R}{T^2} \right)}{\partial \frac{1}{T}} = + \frac{Eg_o}{2} + (E_t - E_i) \tanh Z$$

assuming $E_t - E_i$ and c_n/c_p are not functions of T. From Equation (19), $Z = \pm 1.76$ and $\tanh Z = \pm 0.942$

$$E_t - E_i = \frac{E_{act} - \frac{Eg_o}{2}}{\tanh Z} = \frac{0.317 - 0.392}{\pm 0.942} = \mp 0.0796$$

$$\pm Z = \mp \frac{\left| E_t - E_i \right|}{kT} + \frac{1}{2} \ln \frac{c_n}{c_p}$$

$$\left(\frac{c_n}{c_p} \right)^{\pm 1} = 1.51 \times 10^4 .$$

If

$$c_p > c_n ,$$

then

$$E_t > E_i$$

i.e., E_t is 0.28 v from the conduction band at room temperature.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Chapter 4

STATUS OF THE MULTIPLE DIODE AGING PROGRAM

By G. A. Dodson

4.1 INTRODUCTION

In earlier reports (Refs. 1,2), a multiple diode was described which consists of six computer-type diodes fabricated on one wafer and encapsulated in an eight-pin type 4 header. It was designed as an experimental device which could be used in any circuit which required individual connections to multiple diodes sharing a common output.

After the feasibility stage it was decided to fabricate this device and test its reliability by accelerated aging techniques including step-stress aging (Ref. 3).

Two hundred of these test devices have been prepared and are now being aged. This report presents the aging results to date.

4.2 TEST DEVICES

These multiple diodes were produced over a period of several weeks, in which time a few minor process changes were necessary. In order to prevent any manufacturing differences from influencing the aging results the complete group of two hundred units were randomized. The devices were then divided into twelve groups of sixteen each.

4.3 THERMAL AGING

The thermal aging results to date are summarized graphically in Fig. 41. The solid data point represents completed data, the open data points are the results of extrapolations based on the data presently available from these groups.

A typical failure distribution for the multiple diodes is shown in Fig. 42. The distribution can be seen to be divided into two parts. The first part consists of about 10 per cent freaks which show a wide spread and a low tolerance to thermal

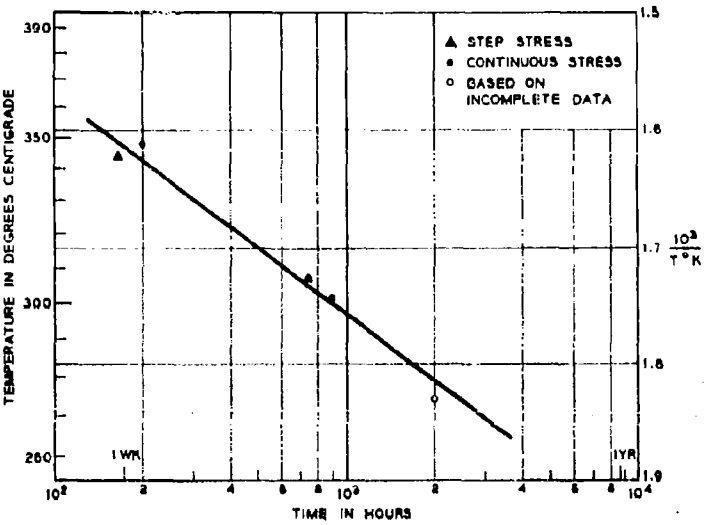

Fig. 41 - Temperature acceleration curve for multiple diodes

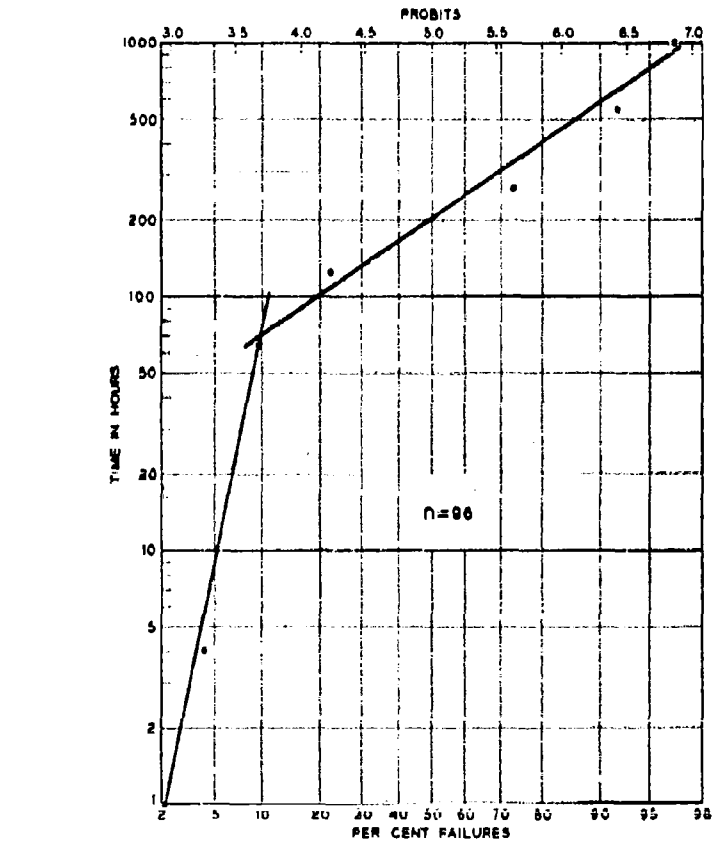

Fig. 42 - Failure distribution for the multiple diodes

stress. The remaining 90 per cent, the main distribution, show a much narrower spread indicating a high degree of uniformity. The main distribution shows an excellent tolerance to thermal stress as indicated by a median failure time of 200 hours at 350°C. In both parts of the distribution an in-can correlation of failures, as reported earlier (Ref. 4), was observed.

4.4 POWER AGING

A twenty four hour power step stress run did not cause 50 per cent failures until the 600 mw level (3.6 watts per encapsulation), at which time most of the failures were caused by open circuits due to burned out leads inside the encapsulation. Further aging tests are being carried out at longer times and/or lower power levels to obtain failures attributable to p-n junction degradation.

4.5 TEMPERATURE AND REVERSE BIAS

A group of units placed on aging at 125°C with 9 volts reverse bias have shown no drifts in 248 hours of aging.

4.6 SUMMARY

The reliability study of multiple diodes is now underway. Present data indicate that the bulk of multiple diodes are remarkably uniform with, however, an appreciable number (~10 per cent) of freaks. These diodes show a high tolerance to thermal and power stress.

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Chapter 5

INTEGRATED SEMICONDUCTOR CIRCUITS

By J. M. Goldey

5.1 INTRODUCTION

The primary reasons which have been advanced for the use of integrated circuits are lower systems cost, improved systems performance and higher systems reliability. In this chapter these "whys" of integrated circuits will be translated into "whats" and "hows".

The problems will be discussed in relation to several specific circuits, in particular a low-level logic gate (Ref. 1). This discussion leads to the suggestion that in a wide variety of digital systems, multiple devices and common encapsulations of different device types go a long way toward meeting the objectives sought by the use of integrated circuits.

5.2 DISCUSSION

One approach to integrated circuits that has been suggested is to use devices which perform functions more complex than those that can be achieved in individual present day devices such as diodes, transistors, etc. When devices of this type become available, they will most certainly find wide application. However, since they are not generally available today, they do not provide the means by which the expected benefits can be realized.

It has also been suggested that the right approach is integration of a small number of standard Boolean circuits from which a variety of systems could and would be built. This approach is different from that mentioned above in that it can be done today. This fact in itself, however, does not justify its use. Such an approach has a number of disadvantages. If the building blocks are designed to render the highest performance in terms of gain and speed needed in the system then the use of these blocks in other parts of the system may be wasteful. If lower performance building blocks are chosen, on the other hand, then it may be necessary to use several of these to perform a function that could have been done with a single high performance circuit. An additional argument against the use of standard building blocks is based on the fact that many subsystem functions can be built with far fewer components if they are designed directly.

In a recent paper, Rice (Ref. 2) has given an example of the difficulties involved when one attempts to build an electronic computer from a few basic building blocks.

The original objective was to design the bulk of the logic circuits for the computer using eight standard Boolean circuit packages. When the drawings were turned over to the manufacturing area, there were, however, 486 instead of eight circuit packages. Although the system could easily have been built using the eight packages, it had better performance at lower cost by using the 486 circuits than it would have had with 8. We may conclude that, at least for many systems, the use of a small number of standard Boolean circuits as building blocks, integrated or not, is not the correct approach.

Before proceeding further, let us consider what is really needed in order to meet the objectives of lower systems cost, improved systems performance, and higher systems reliability.

From the systems point of view, flexibility must be maintained to permit optimum design, to a given performance, if cost reduction is to result. This is almost a truism, yet still not recognized by many. For if standardization on a relatively small number of specific building blocks does anything, it takes away the flexibility of design so vital to the systems designer.

System performance is, of course, determined to a large degree by device performance and, in addition, optimization requires clever circuit design as well. In most systems there are a number of special circuits which require pairs or larger multiples of like devices with closely matched characteristics over wide temperature ranges. Thus schemes of integration which provide devices with such characteristics will lead to better system performance at lower cost. Several examples are described below.

Systems reliability is determined by device reliability and by the margins and redundancy incorporated into the design. Any integration technique, to be useful, must provide reliability at least equal to and preferably better than that which can be obtained by the use of conventional individual components. Of nearly equal importance is the development of reliability evaluation techniques such as stress aging which provide information on failure laws and on the correlation of failures of different devices with usage. Such data will lead to improved systems reliability because it will provide the system designer information which will permit him to optimize his design from margin and redundancy considerations.

From the viewpoint of the device designer, flexibility must also be maintained in order to enable him to take advantage rapidly of important advances in technology. If device manufacturing costs are to be reduced, the use of processes which are not excessively difficult to control is an important factor.

Let us now consider a few examples of integrated circuits which are with us today. They are not sophisticated, but they are, nevertheless, useful, relatively inexpensive, and highly reliable.

As a first example consider a parallel combination of silicon computer diodes (Ref. 3). This multiple diode is illustrated in Fig. 43. A group of six diodes with one side common is fabricated on a common substrate and bonded to a header. Lead wires are attached, by thermocompression bonding in this case, to the individual diodes and the external lead wires. The fabrication procedure for these diodes is essentially identical to that for single diodes of the same type. The only differences are that the die includes six diodes rather than one and that a large central mesa is included so that header bonding may be accomplished without contacting any of the

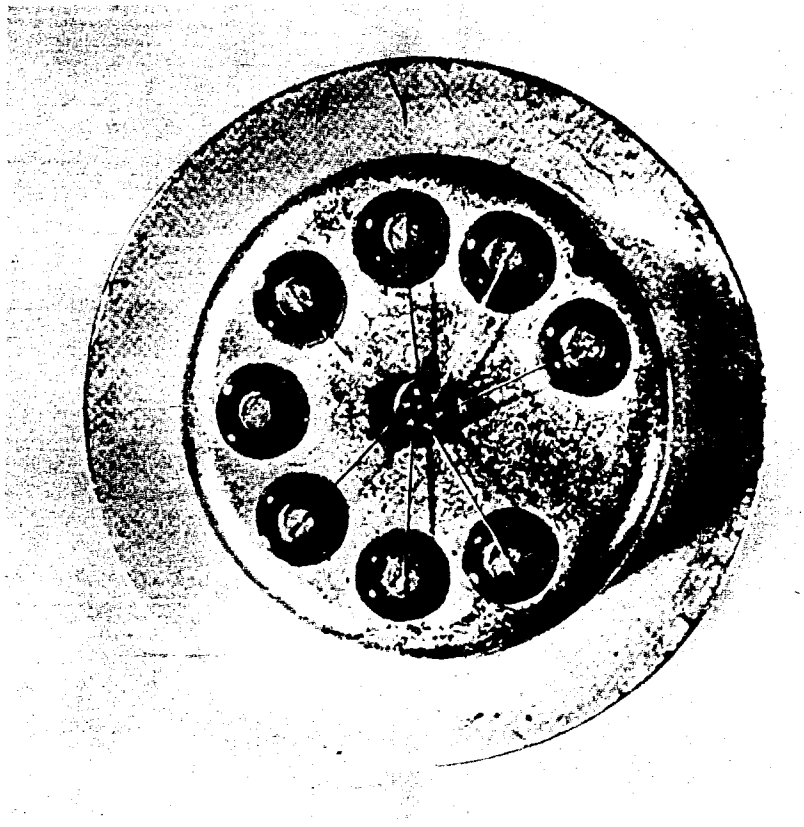


Fig. 43 - Multiple diode. This illustrates a multiple of six silicon computer diodes fabricated on a common substrate. Lead wires are thermocompression bonded to the mesas and to the external leads of the eight-pin header. The larger mesa in the center is used only in bonding the wafer to the header

electrically active regions. A major advantage lies in the use of a single header which one expects to lead to lower costs. In order to realize this benefit, however, a satisfactorily high yield must be achieved. Laboratory results (Ref. 4) have shown that this can be the case and, more specifically, that the yields are much higher than would be expected if dropouts were statistically independent. For statistical independence of dropouts, the yield of a multiple of six diodes would be equal to the yield of the diodes tested individually raised to the sixth power. Actual yields on the above multiple diodes (6 out of 6) have run about Y^3. The reasons for this improvement are clear. The diodes in the multiple are immediately adjacent to one another through all stages of fabrication and thus receive common processing throughout manufacture. Furthermore, some of the major factors controlling yield are functions of the encapsulation process and not of the individual diode.

Results of stress aging of these diodes have been described recently by Howard and Hare (Ref. 5). The important results of that report were that:

(1) The reliability of multiple diodes is approximately equal to that of single diodes of the same type.

(2) That all diodes within a common encapsulation fail at essentially the same stress level.

(3) That failure, when it does occur, is most likely caused by contamination arising from the can itself.

These results imply that no reliability penalty is incurred and that the opportunity for a systems reliability improvement is present.

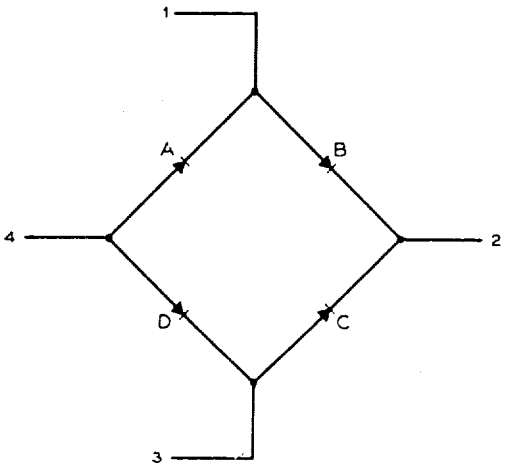
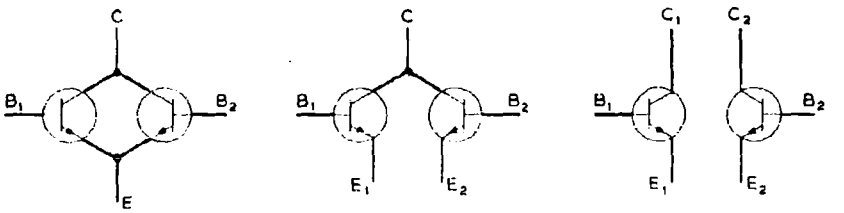


Fig. 44 - Diode bridge circuit. When used as a modulator the performance of this circuit is determined by the match of the forward characteristics of diodes A and D and of B and C. Values of match in forward voltage required vary from 0.1 mv to 100 mv depending on the application.

Another diode example is in order. Fig. 44 shows a bridge circuit which is commonly used as a modulator. The performance of this circuit is determined by the closeness of the match between the forward characteristics of the diode pairs. It has been common practice for several years now for device manufacturers to make individual diodes and then to search for matching pairs by the very laborious method of measuring and cataloguing large numbers of diodes. Once found, matching pairs are packaged together as a unit. Currently, laboratory made multiple diodes are being evaluated for suitability as elements in bridge circuits. Preliminary results, based on a sample of 100 cans, six diodes per can are as follows. For a random choice of two diodes per can, the median difference in forward voltage is 4.3 mv and 88 per cent of the pairs have a difference of less than 10 mv. For the best matched pair in each can, the median difference is 0.35 mv in forward voltage; 100 per cent of the pairs are matched to 10 mv and 82 per cent to 1 mv. In addition to the close match at room temperature, a good match over a wide temperature range is expected because of the intimate thermal contact between the diodes of the pair.

The usefulness of multiple devices is by no means restricted to single junction diodes. As another example consider transistors, which are already being packaged as multiples in a variety of configurations. Several examples are shown in Fig. 45 including an "or" gate where both emitters and collectors are tied together, a chopper where collectors are tied together and a differential amplifier where all leads are brought out independently. In most of these configurations, the closer matched the characteristics of the two transistors, the higher the performance of the circuit.



(a) "OR" GATE (b) CHOPPER (c) DIFFERENTIAL AMPLIFIER

Fig. 45 - Transistor multiples. (a) "OR" gate common to many logic circuits. The emitters and collectors of the two transistors are connected together while the base leads are separate. (b) Chopper used to convert dc to ac. In this case the collectors are common while both emitters and bases are brought out separately. (c) Differential amplifier where all leads are brought out independently.

Improved performance at lower cost results by using two transistors fabricated together and mounted in the same package.

The pnpn diode, one of the few devices currently available, incidentally, which performs a complex function directly, will serve as a final illustration of the multiple device. In one type of electronic switching system under development, switching is carried out on a time division basis. In such a system, high speed, low loss switching elements are needed as gates. An attractive solution consists of a pair of pnpn diodes connected as shown in Fig. 46. Since the diode pair always appears in the same configuration, they can be fabricated in a common encapsulation to reduce the number of cans, thus hopefully reducing the cost, without impairing system performance.

In some of the examples of multiple devices that have been described, there was at least one common connection between different devices, thereby facilitating use of a single substrate. By using this type of multiple, the advantage of elimination of some interconnections is achieved. In some of the transistor multiples and in the pnpn diode, on the other hand, fabrication on a common substrate is difficult and therefore not done.

It is important to realize that different elements need not be on the same semiconductor substrate. Although fabrication on the same slice of material leads, in certain instances, to the elimination of interconnections, the multiple use of single

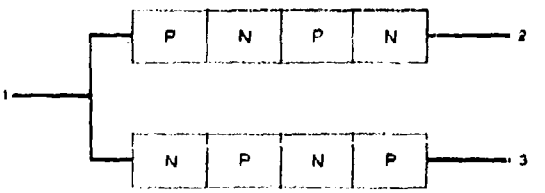


Fig. 46 - PNPN diode gate. PNPN diodes connected as shown provide high-speed, low-loss switching elements for time division gates. The occurence of diodes in pairs, as shown, suggests a common, three-leaded encapsulation for the two devices.

material is advantageous only when the complexity of the structure is not increased and the performance of the circuit is not degraded. In other words the material that is optimum for one device or one function is not necessarily optimum for all devices or all functions. Thus, because a common substrate necessitates the use of a common material, this will also not always be optimum. In particular, one can consider the use of a semiconducting substrate as an insulator to provide isolation between devices and as a resistor.

Further, since the major advantages of integrated circuits come from the use of a common encapsulation it would appear to be sensible to encapsulate different types of devices in a common package without regard to whether or not they are on a common substrate. Indeed, such a scheme is highly desirable in many instances.

Now let us examine a particular circuit and see how these concepts can be applied. The circuit is the diode transistor logic gate known also as LLL or Low-Level Logic. The basic circuit configuration is shown in Fig. 47. The basic features of this logic circuit are as follows:

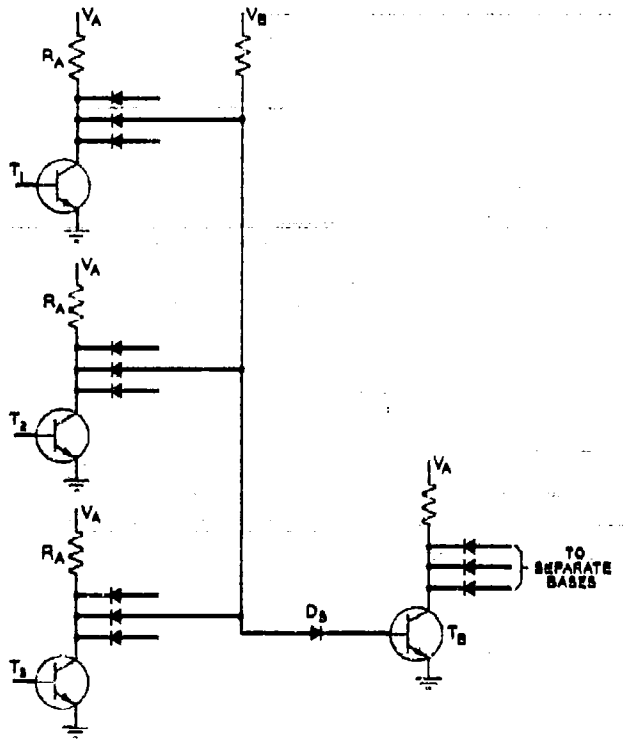


Fig. 47 - LLL gate. This logic gate performs the "and not" Boolean function and in addition provides pulse amplification. If all of the transistors T_1 - - T_N are off, then transistor T_B will be on. If any of the transistors T_1 - - T_N are on, then transistor T_B will be off. The "and" function is performed by the diodes and the inversion or "not" function and amplification by the transistors. The shifter diode D_S provides circuit margin against noise.

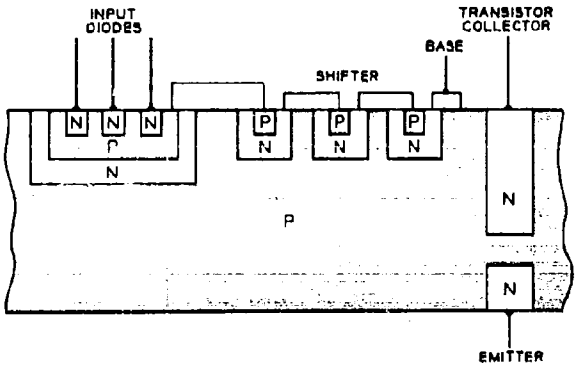


Fig. 48 - Integration of LLL gate on a single substrate. This illustrates how the active components of the LLL gate can be fabricated on a single substrate. Seven diffusion and oxide masking operations plus fifteen lead attachments are required. Performance of such a gate is inferior to one made of individual components and fabrication difficulties are greatly increased.

The input diodes are all connected to collectors of transistors of the previous stage as indicated in the figure. When all transistors connected to these diodes are in their off, or high impedance state, then current will flow from supply B through the shifter diode D_S (which is incorporated to provide margins and in many cases actually consists of three series diodes) into the base of the next transistor turning it on and thus forward biasing all the diodes connected to its collector. This in turn robs the base current of the next set of transistors turning them off, etc. The function performed by this circuit is referred to as an "and not" function, since, when transistor 1 and transistor 2, etc. are off, then transistor B will not be off. In this circuit the diodes are the logical elements and the transistors serve as pulse amplifiers and inverters.

Let us now consider several approaches which might be employed to integrate this circuit. To begin, it is desirable to have at hand some additional information from the circuit designer concerning the specific use of the gate and its many variations. When one examines the use of this logic scheme in any real system, one finds that the number of diodes feeding into any pulse amplifier, called the "fan-in" in circuit parlance, and the number of output diodes, called the "fan-out", varies widely. In typical computers, the fan-in and fan-out may vary from one to ten throughout the system. Therefore any integration scheme that will leave the system designer flexibility must be capable of providing from one to ten diodes per gate. Further examination of the LLL circuits show that the shifter diode never appears in the circuit except in the input lead to the transistor, the base in this case.

Now for the possible methods of integration of this circuit. There are, of course, a considerable number of ways of doing it, but we shall consider only four here. One method consists of complete integration and two ways of doing this are illustrated. First, one could integrate fully on a single substrate of silicon. One method of doing this, chosen for the purpose of illustrating disadvantages as well as advantages, and not because it is the simplest or best way, is shown in Fig. 48. The lines on the figure indicate leads either going to external connections or providing internal inter-

connections. Planar technology permits many of these leads to be made by evaporation of metal films over an insulating layer so that internal interconnections need not be made by thermocompression bonding. In order to provide electrical isolation between the p-side of the input diodes and the transistor base, an n-type region is interposed. The junctions formed between the n-side of the shifter diodes and the transistor base are back biased in circuit use and therefore dc isolated, but their presence does give rise to extra capacity. This scheme provides, through the use of a common substrate, the advantage of either elimination of or easier methods of fabrication of interconnections. However, the yield picture on complex structures is not yet clear and it appears possible that the advantages to be gained could be outweighed by the fact that any defective component requires the replacement of the complete structure. The loss of the ability to pretest and select components for performance is severe and may lead to difficulties, when high performance circuits are fabricated in this manner.

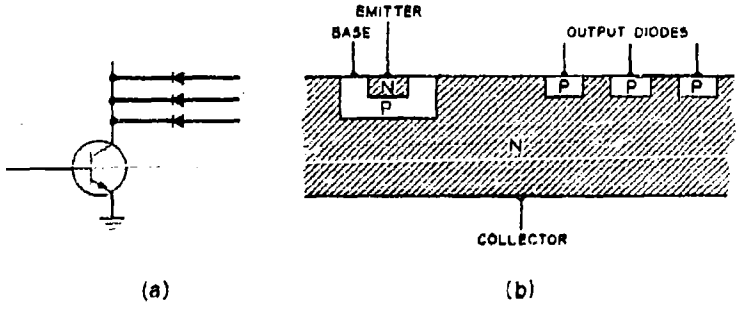


Fig. 49 - Partial integration of LLL gate on a common substrate.
(a) Illustrates the transistor and the output diodes of the LLL gate.
(b) Shows how the transistor and diodes may be fabricated on a common substrate. Use of a common substrate here introduces negligible fabrication difficulties and provides the advantage of elimination of interconnections between the transistor collector and the diodes. Circuit considerations dictate against the general use of this scheme.

Before the second method of fabricating the complete circuit is described, consider another scheme where part of the circuit is integrated on a common substrate. This is illustrated in Fig. 49 which shows the transistor and the output diodes fabricated on a single piece of silicon. This scheme appears to offer advantages because the n collector and the n-side of the diodes are connected together in the circuit, and therefore, fabrication on a common substrate eliminates interconnection without introducing difficulties. In this scheme, the gate could be completed by adding the shifter as a separate wafer and encapsulating all in one package. One disadvantage of this scheme, however, not immediately apparent, does come to light when it is regarded from the systems point of view. The external lead wires connecting the different packages will be from the computer diodes to the shifter diodes. This is the worst place for long leads from noise considerations. Thus, though this is indeed a useful scheme, some price may be paid in system performance and reliability because of decreased circuit margins.

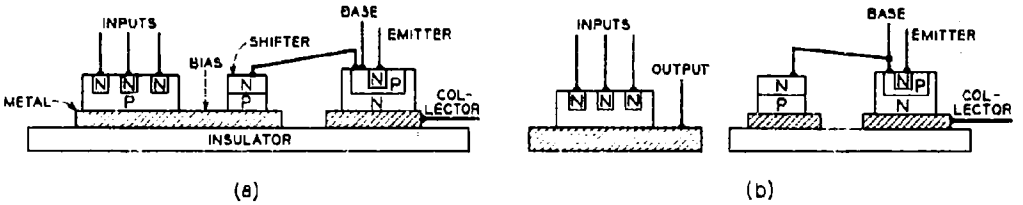


Fig. 50 - Integration of LLL gate with different devices on different semiconductor wafers. (a) Shows integration of the complete LLL gate. The computer diodes are fabricated on a common substrate, the shifter diode and the transistor separately. All components are packaged together. (b) Shows separate packages for the computer diodes and the shifter-transistor combinations.

The next scheme illustrates the second method of complete integration, but no longer on a common substrate. Fig. 50 shows the diodes fabricated on a common substrate, a second wafer for the shifter and a third for the transistor. Again, common packaging is used so that the advantages of potential cost reduction, increased performance and higher reliability are gained and this is accomplished without forcing different types of components onto a common substrate. The fourth scheme also shown in the illustration differs only in that the diodes are in one package and the shifter and transistor are packaged together in another.

Which of these integration methods is preferred when cost, performance, reliability and circuit flexibility (many different values of fan-in in this case) are taken into account? The first two schemes make use of a single semiconductor wafer for either the complete gate or at least a substantial part of it. While offering many advantages, the complexity of the fabrication procedure in the first case and the degradation of performance in the second tends to rule these out at present. Lack of sufficient data precludes a definitive choice between the third and fourth method at this time. However, some of the factors which will influence this choice can be named.

Spare parts are always needed and are usually carried in inventory by both the systems users and the device manufacturer. One such factor is the cost differential between an inventory of complete gates and one consisting of multiple diodes and shifter-transistor combinations. If complete gates are packaged, the inventory cost per package will be higher. On the other hand, if inventories of diodes in single and multiple up to say ten are carried separately from the shifter and transistor package, then more packages may be required, though they will be cheaper. In addition to inventory, other considerations of importance are cost of manufacture and the mechanics and cost of interconnection at the next level. An additional factor relates to the circuit design itself. Should the circuit design be modified in such a way that several stages of diode logic occur without pulse amplifiers and inverters then the separate package method would be desirable. Other considerations will most certainly enter, but these appear to be important ones.

The arguments presented and examples cited above have been primarily concerned with the methods to be used in fabricating the semiconductor components of an integrated circuit. The same line of thought applies equally well, with appropriate modifications, to passive components. It follows that the fabrication of resistors and capacitors of silicon, or other semiconductor material, should be

done only if a performance, reliability or cost gain is achieved. Although semiconductor resistors and capacitors may find application in integrated circuits, in many cases their inclusion leads to a degradation in over-all circuit performance.

5.3 SUMMARY AND CONCLUSION

In this chapter, various approaches to integrated circuits have been discussed and evaluated with regard to their capability to provide lower systems cost, improved systems performance and higher systems reliability. It was also considered necessary that these objectives must be met without loss of flexibility in either systems or device design. Lastly it was recognized that devices which are needed in large numbers and which are not excessively difficult to fabricate are required to give lower costs.

Consideration of devices which perform complex functions directly was limited because they do not, in general, exist. Subsequent considerations of integrated circuits showed that the major advantages to be realized come from the use of a common package rather than a common substrate. Further, the use of a common substrate for its own sake can, in many instances, lead to increased cost with no apparent gain in either performance or reliability.

It was also concluded that integrating Boolean functions has its shortcomings because it limits the systems designer's flexibility. On the other hand, the use of multiple devices and the common encapsulation of different device types go a long way toward meeting the objectives for a wide variety of digital systems.

In summary it is believed that the very real advantages to be gained from the use of integrated circuits can be realized without resorting to over-sophisticated approaches which may instead defeat the intentions.

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2. R. Rice, "A System Designer Views 'Micro-Integrated Electronics' ". Paper presented at the 1961 Solid State Device Research Conference, Palo Alto, California, June 26, 1961.
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Chapter 6

EXPERIMENTS IN THE AGING OF CONTACTS TO SEMICONDUCTOR DEVICES

By G. A. Dodson and B. Stauss

6.1 INTRODUCTION

During accelerated thermal aging experiments performed on transistors (Refs. 1, 2, & 3), a mechanism of failure was observed which is related to the deterioration of the metal to metal bond made to the semiconductor material. This failure mechanism proceeds at a rate sufficient to seriously limit the ultimate life of the semiconductor device and also imposes limitations on the maximum temperature at which some process steps can be carried out. It is the purpose of this Chapter to discuss the results of a series of thermal aging experiments carried out on several metal to aluminum bonds.

The poor aging behavior of these metal to aluminum bonds is revealed in two ways during elevated temperature aging.

1) The resistance of the bonds increases with time.

2) The bonds become intermittent and then complete open circuits.

6.2 TEST DEVICE

In order to study this failure mechanism, it became necessary to make measurements on specially prepared test vehicles. These test vehicles consisted of two metal wires of the appropriate material thermocompression bonded to an aluminum layer which had been evaporated onto a p-type germanium substrate. This structure was mounted in a tubulated type TO-28 transistor encapsulation. Such a structure is free of any p-n junctions which might interfere with measurements of the contact resistance.

Four kinds of metal wires were used in preparing eight groups of devices for this study. The eight groups are:

Group No. 1 - Gold wire units in an open tubulated can.

Group No. 2 - Gold wire units sealed in room air.

Group No. 3 - Silver wire units in an open tubulated can.

Group No. 4 - Silver wire units sealed in room air.

Group No. 5 - Copper wire units in an open tubulated can.

Group No. 6 - Copper wire units sealed in room air.

Group No. 7 - Platinum wire units in an open tubulated can.

Group No. 8 - Platinum wire units sealed in room air.

The open devices were intended to show the effect of aging in a dry air ambient (i.e., that in a clean aging furnace) while those which were pinched off in room air (approximately 50 per cent R.H.) were intended to show the effect, if any, of a limited ambient and/or contamination from the outgassing of the can.

6.3 AGING CONDITIONS

Six units from each of the above groups were placed on aging at each of the following temperatures, 200°C, 250°C, 300°C and 350°C. Such an array of temperatures was chosen in an effort to determine the effect of temperature on the rate of deterioration of the metal to metal bonds.

6.4 MEASUREMENTS

The "soundness" of these bonds was monitored by resistance measurements made through the two metal to aluminum bonds.

6.5 EXPERIMENTAL RESULTS

The aging behavior of the units prepared using silver wires (Groups 3 and 4) is very poor with the bonds becoming open circuits within the first ten hours of aging on most of the aging runs. However, the cans which were left open tended to

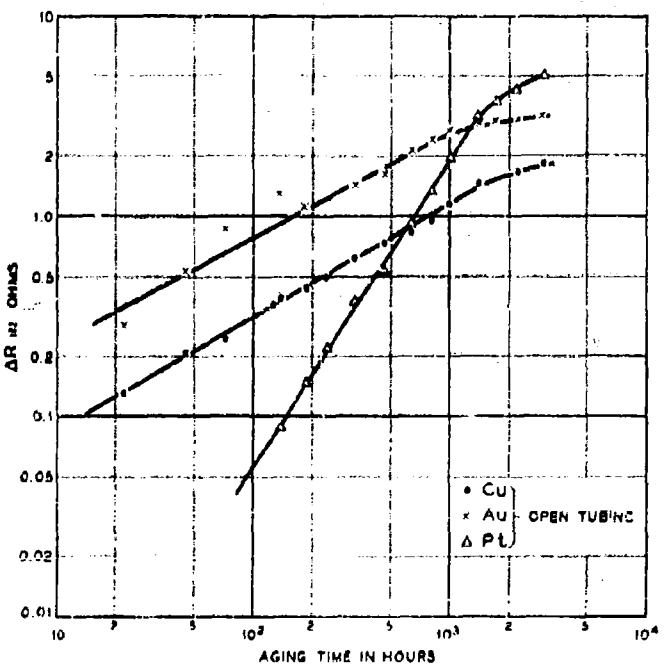

Fig. 51 - Aging characteristics of bonded wires (Aged at 200°C)

outlast the sealed units. Because of the insufficient data on these units, they will not be considered in the results to follow.

Fig. 51 shows typical resistance changes versus aging time for open cans (Groups 1, 5 and 7) aged at 200° C. All other experimental groups and/or aging conditions show a similar trend with more pronounced resistance change.

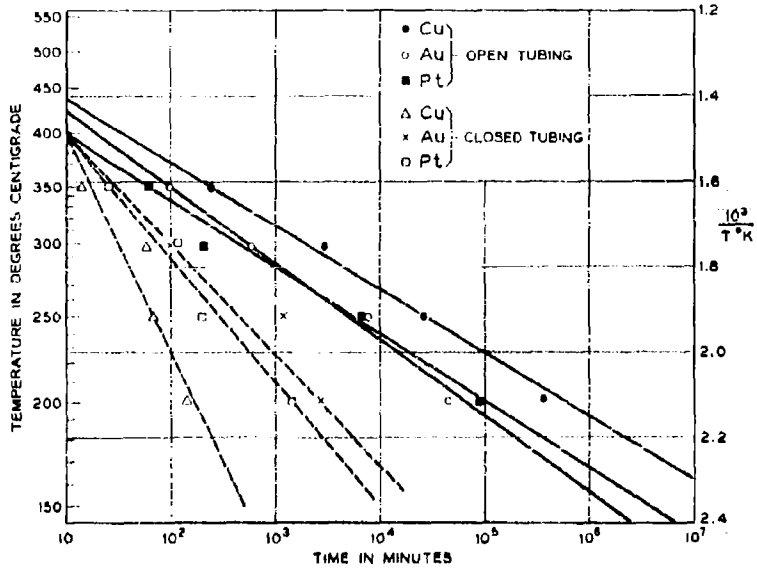

Fig. 52 - 50% bonded-wire failures (Failure $\Delta R \geq 2$ ohms)

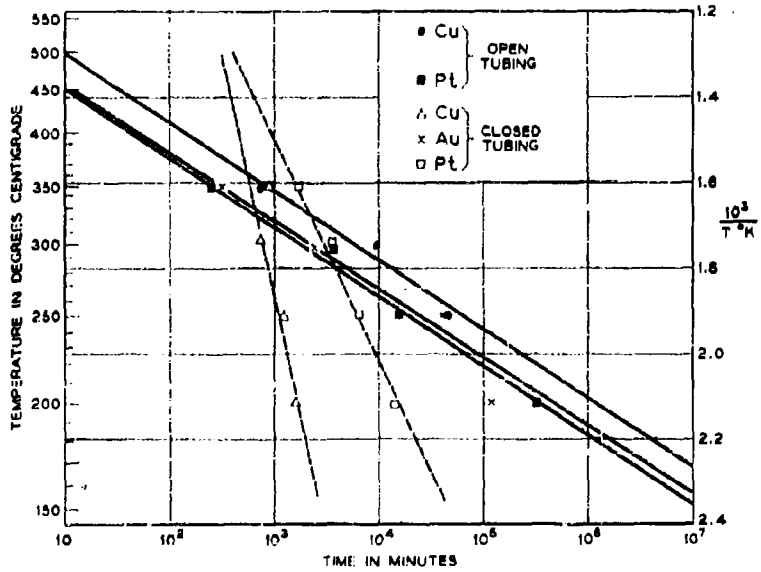

Fig. 53 - 50% bonded-wire failures (Failure $\Delta R \geq 100$ ohms)

Figs. 52 and 53 show, graphically, the results of resistance change as a function of the aging temperature of Groups 1, 2, 5, 6, 7, and 8 for two-ohms increase and one-hundred ohms increase respectively.

It should be noted from these figures that the sealed units (Groups 2, 6, and 8) have much shorter aging life then the units left open to air.

6.6 CONCLUSIONS

An important mechanism of failure of germanium transistors as a result of thermal aging is a change in resistance in the electrode connections together with a reduction in the mechanical strength of the lead bond. It is believed that the mechanism of this failure is related to the solid state diffusion, surface or bulk, of the various elements present.

This failure mechanism imposes a serious limitation to the reliability of the devices. Since this is a problem of major importance, it is proposed that additional experiments be directed toward confirming the postulated mechanisms. By such a program it is expected that solutions can be found to remove this restriction on the performance of these devices.

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2. L. E. Miller, and I. M. Mackintosh, in "Semiconductor Reliability," Reinhold Publ. Corp., N. Y., N. Y., 1961, Chapter 8.
3. L. Bernstein, Semiconductor Products, July-August 1961, p.

SECTION 5 - CONCLUSIONS

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

The fabrication of the desired surface geometry for the 1-watt, 1000-mc transistor, using the new techniques of oxide stripe separation, has been carried out. Some modification of jigging and processing must be done before devices can be produced. Further characterization of mesa transistors indicates that the base resistance of the device is at least as low as the value computed from its structure. Further reduction of the encapsulation parasitic inductances must be obtained before unambiguous evlauation of the transistor wafer may be obtained. Higher collector-breakdown voltage must be obtained to meet design objectives.

Design calculations indicate that a low-power transistor with a unilateral gain of 14 db at 3 kmc is feasible. A 0.25-mil diameter emitter, with 0.1-mil separation between the emitter and base electrodes, is necessary. Structures of this size have been produced. However, scattering of the evaporated materials during the evaporation of the electrode structure has prevented fabrication of satisfactory devices. A new low-parasitic encapsulation is also necessary for this device.

The low-frequency base current in all diffused-base germanium transistors, which results in a fall-off of current gain at low emitter currents, appears to be due solely to a surface recombination current in the emitter space charge at the perimeter of the emitter electrode.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Early results from a series of accelerated aging experiments on multiple diodes in a single encapsulation have indicated that the main population (90 per cent of the units) possess good tolerance to both thermal and electrical stresses. The remaining 10 per cent are statistical freaks showing power aging properties.

A review of various methods of integrating semiconductor circuits led to the conclusion that integration on a single substrate, or the integration of solely Boolean functions, possesses disadvantages. An approach utilizing multiple like devices on a common substrate and the common encapsulation of unlike devices on separate substrates appears to go a long way toward meeting the objectives for a wide variety of digital systems.

Accelerated aging experiments on thermal compression bonded lead wires to aluminum contacts on a semiconductor substrate have shown that the resistance of the bond increases until an open circuit occurs. The rate of aging appears to be a function of the ambient atmosphere around the bond.

SECTION 6 - PROGRAM FOR THE NEXT INTERVAL

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

The fabrication of the 1-watt, 1000-mc transistor with the new structure will continue, and processing details will be improved, so the completed devices can be obtained. Additional evaluation of both the new structure and the mesa structure will be carried out to obtain a better understanding of the device. An effort will be made to improve the quality of the epitaxial germanium in order to increase the collector breakdown voltage.

Investigation of scattering of evaporated materials will continue as the major effort on the small geometry necessary for the M2275 transistor. Work on evaporation masks and jigging will continue with the goals of improving the geometry and easing the device fabrication.

Design studies for both devices will continue and fabrication of very low parasitic encapsulations for both devices will be started.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

The development of the technology necessary in the production of integrated circuits will be continued. Particular attention will be paid to the establishment of integration techniques possessing the flexibility necessary for wide application to various digital systems.

Accelerated aging studies will continue to investigate the mechanisms of failure associated with semiconductor devices.

Experiments to determine the reliability of multiple diodes in a single encapsulation will be completed and the results will be evaluated.

SECTION 7 - IDENTIFICATION OF PERSONNEL

ARTHUR G. FOYT

Arthur G. Foyt received the degree of Master of Science in Electrical Engineering from the Massachusetts Institute of Technology in June 1960.

He joined Bell Telephone Laboratories in July 1960, where he has worked on germanium mesa transistors.

JAMES M. GOLDEY

James M. Goldey received his Ph.D. in physics from M.I.T. in 1955. While at M.I.T., he measured the effective masses of electrons and holes in germanium. Upon joining Bell Telephone Laboratories in 1955 he worked on the development of evaporation and alloying techniques of various materials to silicon. More recently he has worked on the development of diffused silicon transistors and pnpn devices. He is now a Department Head responsible for activities in silicon transistors, integrated circuits, and pnpn and functional devices. He is a member of the Institute of Radio Engineers, the American Physical Society, Sigma Xi, and Phi Kappa Phi.

ALAN B. KUPER

Alan B. Kuper received his B.S. in Physics from the University of Chicago in 1949 and his Ph.D. in Physics from the University of Illinois in 1955. His work in experimental metal physics was continued at Princeton University, before coming to Bell Telephone Laboratories in 1957. Since then he has been engaged in diffusion, alloying and materials studies connected with diffused-base germanium transistor development. He is a member of the American Physical Society.

B. STAUSS

B. Stauss joined Bell Telephone Laboratories in 1930. Until 1940, he was engaged in the development and testing of circuit components. During the war years, he worked on the design of an electromagnetic mine detector. From 1945 to 1956 he was concerned with the design and testing of electrochemical switching apparatus. From 1956 to the present, he has been concerned with various phases of semiconductor development. He received an E.E. degree from the Cooper Union in 1939.

Earlier reports under this contract and its predecessor contracts have identified other engineers and scientists whose work has contributed materially to this program.

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Contract DA 36-039 sc-88931 (Unclassified)

Prepared by: R. E. Davis, J. M. Goldey, G. A. Dodson, B. T. Howard, A. G. Foyt, A. B. Kuper, B. Stauss

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The general objective of this contract is to make studies and investigations related to transistors and transistor-like devices, with a view toward demonstrating and increasing the practicability of their use in operating equipment.

This report covers the status of work on microwave germanium transistors and on integrated circuit devices. Experimental and calculated performance data are given for a low power 3Gc and a 1-watt 1 Gc transistor. A review of various approaches to integrated semiconductor circuits leads to the conclusion that most gains will be obtained through a flexible approach using multiple like devices on a common substrate and the common encapsulation of unlike devices on separate substrates. Some aging and reliability results are discussed.

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2. DA 36-039 sc-88931

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Period 1 October to 31 December 1961.
Contract DA 36-039 sc-88931 (Unclassified)

Prepared by: R. E. Davis, J. M. Goldey, G. A. Dodson, B. T. Howard, A. G. Foyt, A. B. Kuper, B. Stauss

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